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Conducted Emission Suppression Using an EMI Filter for Grid-Tied Three-Phase/Level T-Type Solar Inverter

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ABSTRACT Electromagnetic interference in power converters is a crucial problem for circuit designers. Electromagnetically compliant converter design is required for the safety of an operation. A novel filter design approach considering ground leakage current, different winding styles for common mode choke, tolerance of filter capacitor is proposed in this study to solve the electromagnetic interference problem. In the study, electromagnetic compatibility issue is investigated for a 25 kW, 15 kHz switching frequency, three-phase/level T-type grid-connected solar inverter. The test setup is installed based on EN55011 standard, and the interferences emitted by the inverter to the grid through conduction are measured. Then, a filter design is made to prevent these interferences from being transmitted to the grid. After the filter is designed and engaged, the measurements are repeated. So, the noise attenuation of the EMI filter is verified experimentally. Experiences obtained from the hardware modification in the EMI filter, which is designed for an industrial solar inverter, have been discussed. It is observed that the result of conducted emission measurement is within the limits of the EN55011 Class B standard.

INDEX TERMS Electromagnetic interference, electromagnetic compatibility, EMI filter, solar inverter, common mode, differential mode.

I. INTRODUCTION

Inverters are power electronic circuits that have an essential role in connecting renewable energy systems to a grid. Grid-connected transformerless solar inverters have drawn attention due to their high power density, high efficiency, and low cost. With advanced semiconductor technology, high power density and low volume in circuit design are achieved by switching the elements of inverter circuits at higher frequencies. High switching speed causes high electromagnetic radiation, which causes electromagnetic interference (EMI). Industrial product designers must meet the electromagnetic compatibility (EMC) conditions described in relevant regulations and standards to ensure that the products are made electromagnetically compatible with their environment.

The basic approaches in the literature to reduce EMI and to meet EMC standards are intervening at the source of interference (soft switching, random modulation, and PWM control) and preventing the interference path (EMI filter and EMI shielding) [1].

In the first approach, it is possible to reduce the noise with the changes made on the circuit without using additional elements. In the second approach, EMI filter design is required to attenuate undesired interference by building impedance on the interference path [2], [3].

There is a great effort to build the EMI noise model for the power electronic converters. It is a useful approach for determining the noise level and finding the appropriate filter design for noise attenuation. The basic method in solving the EMI problem is to determine the sources and the paths of interference by extracting the high-frequency model of the circuit. Thus, time-domain and frequency-domain modeling approaches are used in EMI design.

On the one hand, the time-domain modeling is conveniently applicable, but on the other hand, it is computationally complex. It should be kept in mind that it is a time-consuming approach, especially when small time intervals are used to improve the model's accuracy. Although the knowledge

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of the noise source and interference paths is required in frequency-domain modeling, it is still a highly preferable approach compared to time-domain modeling. Because it significantly reduces the computational complexity. The success in solving the EMI problem depends on the creation of an accurate model of the noise source and interference paths. The fundamental logic in frequency-domain modeling is to model the noise source (switching devices) as a trapezoidal waveform whose characteristic is known in that domain. In frequency-domain modeling, while the switches are replaced with a voltage source, diodes are replaced with current sources according to the substitution theorem.

EMI filter design is a demanding problem for power electronics circuits, and the solution to the EMI problem is unique to the circuit. Therefore, it is necessary to make an appropriate filter design by determining the noise interference paths in the power electronics circuit.

Some studies propose an EMI filter design to mitigate EMI levels below standard limits so far. For instance, the EMI noise model and filter design for a 1 MHz 10 kW three-phase/level PWM rectifier are presented in [4]. The converter's noise model has been created and, in this model, MOSFETs are modeled as a voltage source, and diodes are modeled as a current source. In the article, both CM and DM filter designs have been implemented, and the LCLCL type has been used as the filter topology.

Gulur *et al.* have proposed a CM EMI filter design for three-phase two-level VSC [5]. In the proposed filter design, the heatsink with reference ground connection over impedance provides a return path to CM current, and thus CM noise amplitude is reduced. In heatsinks that are grounded through an impedance, heatsink voltage must be kept close to the ground potential to prevent the heatsink from causing radiated emission (RE) by acting as an antenna. However, there is no RE analysis or measurement support that the proposed design is also valid in RE. Although the proposed filter structure provides diversity in filter design, it comes with additional design requirements such as ground leakage current investigation and heatsink potential calculation.

The impedance balancing method is another method used in EMI filter design. It is an effective method because of its cost and filter size since it does not require too many elements [6]. In the research conducted by Zhang *et al.* [7], the CM noise model has been created for 1 kW three-level/phase NPC topology. The CM noise has been reduced via the noise balancing method by connecting the converter and LCL filter neutrals through an L inductance. However, in this method, there is also a possibility of impedance balance deterioration in industrial applications due to the PV system's uncertain and variable parasitic effect.

In the study conducted in [8], a simulation-based EMI filter design method is proposed for universal converters. CM and DM filter designs have been made on different converters with single-phase and three phases.

CM and DM stages of the EMI filter are determined by using a software-based noise mode separator in a three-phase inverter circuit for the motor driver in [9]. Boillat *et al.* have proposed a two-stage EMI filter design (LCLCL filter) that provides optimal power density for a three-level T-type boost PWM rectifier circuit [10], [11]. In the proposed multi-stage filter design, the ratio of CM inductance to DM inductance in the first filter layer is determined as a parameter. Besides, an approach affecting the total filter volume is presented.

CM noise investigation is conducted on a three-level/phase active neutral NPC (I-type) inverter in [12]. First, the noise sources are determined by establishing the CM noise model of the circuit. Then the noise is reduced by using hardware-based approaches such as adding CM choke, combining the midpoint of the transformer neutral and DM capacitance, adding inductance between the midpoints, adding Y capacitor to the DC bus. Simulation methods in time and frequency domains are given in detail to model the EMI problem of inverter circuits in [13].

The three-terminal model of the three-phase inverter is built, and mixed-mode noise analysis is performed in [14]. However, there is no study conducted towards the filter design. In a study carried out in [15], CE and RE measurements are made for an inverter circuit for on-grid, off-grid, and hybrid operating modes. In the study, interference reduction methods are not mentioned; only measurements are made according to the standards defined for inverters.

In the research conducted by Xiang *et al.* [16], EMI sources are modeled in the frequency domain for two-level three-phase inverter circuits. The study is about extracting the CM and DM noise model, but there was no proposed method for solving the EMI problem. The oscillation effect in deriving the noise model is examined, and its contribution to the model accuracy is determined. In [17], CM noise analysis has been made, and filter design has been proposed for the asymmetric active phase converter circuit feeding a three-phase asynchronous motor from a single-phase network.

Nanocrystalline material-based choke design is compared with ferrite choke in [18] for a PWM inverter-fed induction motor driver to reduce filter size. It is clear that high permeability material selection will reduce the choke size and contribute power density of the motor driver. In [19], an EMI filter is designed with the EE and EIE-type cores. Filter with the proposed choke design provides volume reduction in single and multi-stage EMI filters. The noise source model is not given in these studies.

Several studies have focused on three-phase EMI filter design. However, the EMI filter design for the three-phase four-wire (3P4W) PV inverter has not been investigated. In this study, the detailed examination of the EMI filter design for the 3P4W three-level PV inverter has been presented, and the inverter model in the frequency domain has been created.

In this study, an EMI filter is designed for a T-type three-level, three-phase solar inverter prototype using a 25 kW Si IGBT switch module. In order to ensure the accuracy and repeatability of the measurements, background noise is also considered in the study. The contributions of the study on EMI filter design are listed as follows:

- EMI filter design with high power density for solar inverter application.
- Low ground leakage current level compliant with VDE 0126-1-1 standard.
- Filter design compliant with EN55011 Class B Group I requirements.
- Leakage current calculation is presented by considering the tolerance of filter capacitors.
- The superiority of the EMI filter design is proven by both experimental and simulation results.

The rest of the paper is organized as follows: In Section II, information about the topology of the inverter circuit is given, and equivalent models according to noise modes are presented. Filter arrangement and selection of filter elements have been examined in Section III. In Section IV, simulation and experimental study results are given by taking measurements on the 25 kW three-level/three-phase split T-type inverter prototype. The success of the designed filter has been confirmed. Design problems and solution-oriented approaches experienced in the experimental study are also shared.

II. T-TYPE INVERTER AND NOISE MODELING

A. THREE LEVEL THREE PHASE T-TYPE INVERTER

T-type neutral point clamping (T-type NPC) inverters have recently become popular due to their advantages in areas such as the integration of renewable energy, electric vehicle systems, and motor drive applications. T-type NPC inverter can provide power flow with low total harmonic distortion (THD) at low switching frequencies compared to conventional inverters. In addition to that, it has low voltage stress on switching elements [10], low switching losses, and it requires small filter sizes [20]. If T-type inverters are compared with I-type inverters, it is observed that switching losses are smaller. T-type inverters are preferred in medium and high-power applications such as solar systems, uninterruptible power supply (UPS), motor drives, mostly due to their superiority in harmonics and efficiency.

Studies have shown that T-type topology provides higher efficacy and better AC output voltage waveform with increasing switching frequency [21]–[23]. Although high switching frequency provides high efficiency and power density, it also causes unwanted electromagnetic interference problems. Power density is an important criterion in circuit design. Thus, the EMI filter should be designed optimally because it takes approximately one-third of the inverter's total volume [10]. As an industrial product, it is a legally binding obligation to meet the electromagnetic noise limit values determined by the EMC directives for the inverter.

NXH160T120L2Q2F2SG T-NPC power module of On Semiconductor is used in the prototype design. These modules are mostly used in solar inverter and UPS circuits, which are also called industrially mixed voltage NPC topology. This module is preferred for the solar inverter prototype because it provides convenient gate control by preventing the split output cross-transmission and offering an effective design with low inductive pinout in terms of EMC. In this respect, it is a suitable topology for three-phase solar inverter applications. Also, this circuit is a higher power density optimized version of conventional T-type topology.

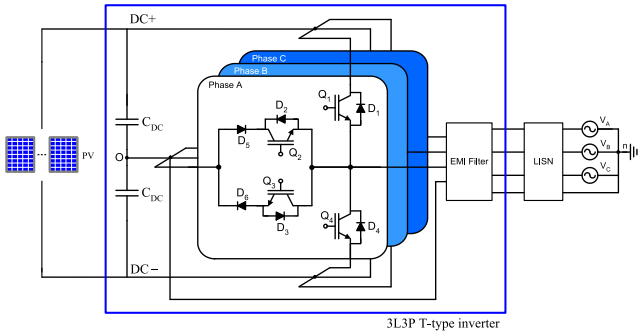


FIGURE 1. Grid-connected three-phase three-level T-type PV inverter.

TABLE 1. Parameters of three-phase/level PV inverter.

Parameter	Value
Grid voltage (V_s)	230 V
Grid frequency (f_g)	50 Hz
PWM frequency (f_s)	15 kHz
Output power (P_o)	25 kW
Output DC voltage (V_{dc})	800 V
Bus capacitance (C_{bus})	0.8 μF

The circuit shown in Fig.1 is a grid-connected split-capacitor three-phase four-wire inverter circuit. Unlike the classical T-type topology, this topology is divided into the high side bridge consisting of Q_1, D_1, Q_2, and D_2 and the low side bridge consisting of Q_4, D_4, Q_3, and D_3 to minimize the inductive loop in the switches. In the topology, D_2 and D_3 protection diodes are used to direct the reverse recovery currents of neutral point freewheel diodes D_5 and D_6. Protection diodes have a smaller forward current than freewheel diodes.

The topology presented in Fig.1 is used in many areas such as photovoltaic systems, active power filters, and electric vehicle battery chargers in which unbalanced voltage/current issues occur. The difference of this circuit from a three-phase-three-wire inverter is that the midpoint of the dc-link capacitors is connected to the grid/load neutral, and a fourth wire is added. Three independent single-phase systems have been obtained from a three-phase system with this connection.

The design parameters of the T-type PV inverter given in Fig.1 are given in Table 1. Also, the efficiency of the designed inverter is measured as 97.5% at 25 kW.

B. NOISE SOURCE AND NOISE MODES MODELING

In EMI filter design, knowing the noise sources and noise modes is necessary to derive the equivalent circuits of the noise modes. A behavioral model of IGBT given in Fig.2 is used for the EMI modeling. As a result of high-frequency switching and high dv/dt and di/dt changes, the inverter

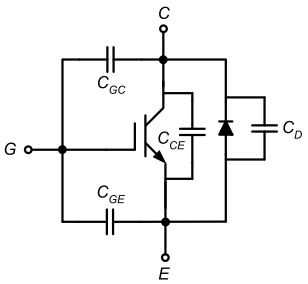


FIGURE 2. The behavioral model of IGBT with junction capacitances.

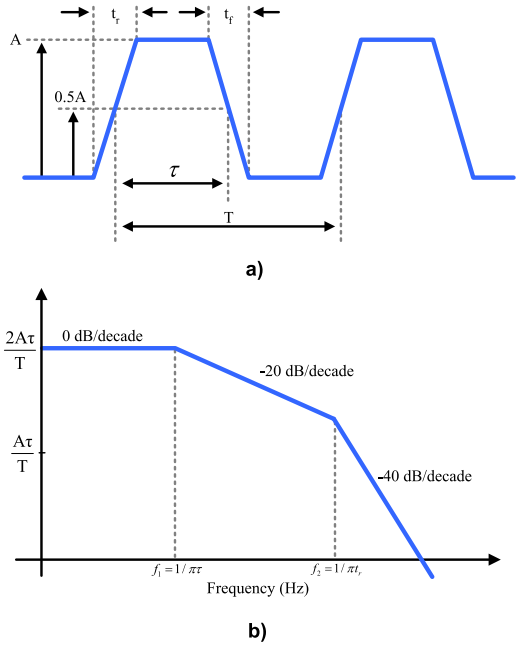


FIGURE 3. a) Trapezoidal voltage waveform b) spectral envelope of the trapezoidal waveform.

becomes a natural source of EMI noise. The dynamic behavioral model of the IGBT module is derived from its datasheet and is used in high-frequency modeling. Following capacitances can be obtained from the datasheet. $C_{ies} = C_{GE}+C_{GC}$, $C_{oes} = C_{CE}+C_{GC}$, $C_{res} = C_{GC}$, where C_{ies}, C_{oes}, and C_{res} are input, output, and reverse transfer capacitances, respectively.

The switching waveform of IGBT can be modeled as asymmetrical trapezoidal pulse as seen in Fig.3(a), and the spectral envelope of this waveform is obtained as Fig.3(b). In this equivalent circuit approach, switching devices (main sources of the EMI) are modeled as the voltage sources with a trapezoidal shape. Developing robust models and reducing model complexity can be achieved through this simplification.

PWM pulse is frequently represented with trapezoidal waveform with a period T, a pulse width (points between 50% of the waveform amplitude) τ, a pulse rise-time τ_r, a pulse fall-time τ_f, and an amplitude A. The trapezoidal waveform envelope is written as (1), assuming that the rise and fall times

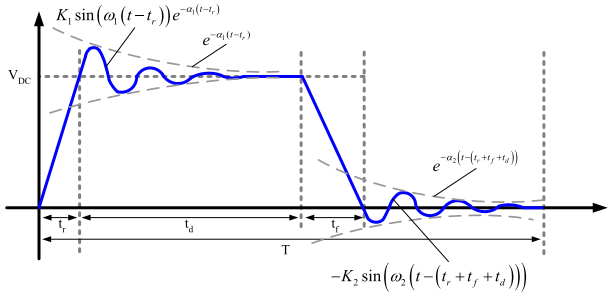


FIGURE 4. Switching waveform of V_{ce} voltage of IGBT.

of the waveform are equal. The logarithm of (1) is taken for the generation of bounds, and as a result, (2) is obtained.

$$Envelope = 2A\frac{\tau}{T}\left|\sin c(\pi\tau f)\right|\left|\sin c(\pi\tau_r f)\right| \quad (1)$$

$$\begin{aligned} 20\log_{10}(envelope) = {} & 20\log_{10}\left(2A\frac{\tau}{T}\right) \\ & +20\log_{10}\left(\sin c(\pi\tau f)\right) \\ & +20\log\left(\sin c(\pi\tau_r f)\right) \end{aligned} \quad (2)$$

where $\sin c(x) = \sin(x)/x$.

It is evident from (1) and (2) that pulses with fast rise/fall times have larger spectral content than the pulses with slow rise/fall times. Increasing rise/fall times is necessary to reduce emissions to meet the regulations of conducted/radiated emission limits.

The approximation of the symmetrical trapezoidal waveform is not adequate to define the real behavior of the switching mechanism and the circuit. Moreover, this approximation can predict the switch behavior with reasonable accuracy. Thus, the ringing effect should also be taken into account to increase the model's accuracy. The general mathematical function of the ringing is defined as in (3).

$$Ke^{-\alpha t}\sin(\omega_r t) \quad (3)$$

where α is the damping coefficient. The envelope of the ringing effect is given below. The approximate switching behavior of IGBT is shown in Fig.4.

The superposition of these three waveforms presented in Fig.4 gives the final model of the switch [24].

$$\begin{aligned} c_n = {} & \frac{V_{dc}T}{4n^2\pi^2}\left\{\frac{1}{t_f}\left(1-e^{-jn\frac{2\pi}{T}t_f}\right)e^{-jn\frac{2\pi}{T}(t_t+t_d)}\right. \\ & \left.-\frac{1}{t_r}\left(1-e^{-jn\frac{2\pi}{T}t_r}\right)\right\} \\ & +\frac{K_1\omega_1}{T\left(C_1^2+\omega_1^2\right)}e^{-jn\frac{2\pi}{T}t_r}\left\{1-\cos(\omega_1 t_d)\,e^{-C_1 t_d}\right. \\ & \left.-\frac{C_1\sin(\omega_1 t_d)}{\omega_1}e^{-C_1 t_d}\right\} \\ & -\frac{K_2\omega_2}{T\left(C_2^2+\omega_2^2\right)}e^{-jn\frac{2\pi}{T}t_0}\left\{1-\cos(\omega_2(T-t_0))\right. \\ & \left.\times e^{-C_2(T-t_0)}-\frac{C_2\sin(\omega_2(T-t_0))}{\omega_2}e^{-C_2(T-t_0)}\right\} \end{aligned} \quad (4)$$

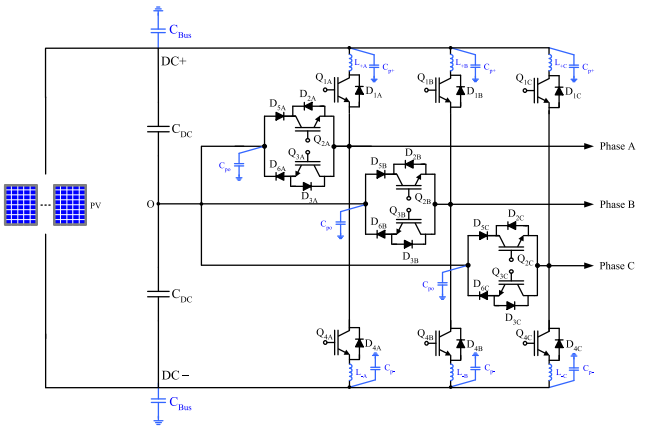


FIGURE 5. Three-phase T-type solar inverter circuit with parasitic elements.

After modeling the switching element as the noise source, parasitic capacitance and inductance knowledge of the inverter can be obtained by measurement. The parasitic elements of the inverter are shown in Fig.5.

C_p is the parasitic capacitance between the heatsink of the switch and the ground. C_{p+}, C_{p-}, and C_{po} are 79.49 pF, 80.86 pF, 182.30 pF, respectively. $L_{-/+X}$ (x defines phase) is the parasitic inductance of the busbar of any phase. The parasitic inductances are obtained as $L_A = 126.8$ nH, $L_B = 184.1$ nH, and $L_C = 153.25$ nH according to the measurement results.

Conducted EMI is divided into two modes according to propagation path: common mode and differential (normal) mode. Common mode (CM), or in other words, asymmetric noise, is generated from potential fluctuation caused by charge and discharge of stray capacitances between the circuit and the ground. CM current flows from the power conductors (phase and neutral) of the device in the same direction and returns to the source through the ground. Differential mode noise (a.k.a. symmetrical noise) is caused by high *di/dt* and *dv/dt* because of IGBT switching, and DM current flows in the opposite direction in the power conductors.

Detection of the CM noise and solution to that problem is relatively more difficult than the DM noise problem in high power converter circuits. Especially in applications with long cable connections at the input and output, such as solar inverters and UPSs, the conducted CM currents will also cause high radiated interference.

Common and differential mode voltages are calculated as in (5) and (6) for the inverter circuit given in Fig.1.

$$U_{CM} = \frac{U_{AO} + U_{BO} + U_{CO}}{3} \tag{5}$$

$$U_{DM} = U_{AB} - U_{CM} \tag{6}$$

Components of common and differential mode [25] are given in (7) and (8).

$$U_{DMi}(t) = \frac{8V_{DC}}{\sqrt{3}\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_n\left(m\frac{\pi}{2}M\right) sin\left([m+n]\frac{\pi}{2}\right) \times \sin n\frac{\pi}{3} cos\left(m\omega_c t + n\omega_0 t\right) \tag{7}$$

$$U_{CMi}(t) = \frac{4V_{DC}}{3\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \frac{1}{m} J_n\left(m\frac{\pi}{2}M\right) \times sin\left([m+n]\frac{\pi}{2}\right) \times \left[1 + 2cosn\frac{2\pi}{3}\right] \times cos\left(m\omega_c t + n\omega_0 t\right) \tag{8}$$

where i = A, B, and C phase legs

m, n: harmonic indexes

$J_n(x)$: Bessel function of order n with argument x

ω_c: angular frequency of carrier waveform

ω_0: angular frequency of fundamental component

M: modulation index

Frequency spectrums of noise sources are used to predict the noise modes accurately. CM noise attenuation is relatively more difficult than DM noise. Because every element that has a connection with the ground can create an interference path in CM noise. The CM voltage will cause the CM current to flow in the neutral line. In addition to the three-phase windings of the CMC, there is a winding for the neutral connection to weaken the CM current. Thus, the inductance added to the neutral will increase the CM impedance, and the CM current will be reduced. CM noise is also reduced by connecting the neutral point to the star point of the DM capacitors. Also, it has been observed that the noise is further reduced by combining two points over an impedance [12]. In a study based on this issue, it is observed that CM noise can be reduced by combining the star point with the O point, which is the midpoint of the capacitor in EMI filter design [26].

III. EMI FILTER DESIGN

Power conversion with inverter or rectifier circuits produces high-frequency noise. For this reason, three-phase EMI filters are particularly important in reducing electromagnetic interference in three-phase applications, preventing interferences that hinder devices from reliable operations, and ensures companies to comply with the EMC regulations.

Three-phase EMI filters are designed to meet the requirements of EMC regulations specified for industrial applications. In the relevant EMC regulation, the maximum allowable noise level transmitted to the power line in each frequency range is given in dB. Three-phase wye EMI filters are designed for switching power conversion devices and applications requiring a neutral connection. The advantage of these filters is that they save money in terms of cost and filter space, thanks to the need for a lower voltage capacitor than delta filters. These filters can also be used for unbalanced loads by grounding the star point.

A. EMI FILTER LAYOUT AND ELEMENT SELECTION

The elements used in EMI filter design are CM choke and Y capacitor for common mode, DM inductor, and X capacitors for differential mode. In EMI filter design, each filter element can theoretically filter 20 dB/decade of noise. However, in the real case, filtering happens to be lower than the ideal

value since the filtering effect decreases due to the parasitic parameters of the filter element.

1) EMI FILTER LAYOUT

EMI filter design is made with the acceptance that source and load impedances are compatible at 50 Ω as in communication systems and microwave applications. For this purpose, 50 Ω load impedance condition is provided by line impedance stabilization network (LISN). In real applications, the load impedance corresponds to the network impedance, while the source impedance is the equivalent impedance seen when looking towards the device side. These two impedance values are not 50 Ω, and it is uncertain that they will remain constant in the frequency range measured for the CE test [27].

The main purpose of impedance mismatch in EMI filter design is to provide impedance discontinuity in the transmission path of the high-frequency electromagnetic signal. Thus, most of the electromagnetic signal is reflected on the source. Reflection will occur if the output impedance of the filter is not equal to the load impedance. When the impedance mismatch is achieved at the input and output of the filter, the noise signal will be reflected on its input and output connections [28].

When the filter structure is not considered according to the impedance mismatch, it is seen that more filter elements are required to attenuate the same noise. Besides, there is an increase in the size of the filter elements. This indicates a poor design in terms of cost and power density which is not desirable for filter designers.

The expected filter attenuation is determined by modeling the insertion loss of the selected filter topology. In the traditional approach, the insertion loss of the filter is measured by assuming that there is a fixed 50 Ω impedance at the filter input and output for CM and DM modes. However, the impedances are uncertain and differ according to the application. For this reason, measurements should be made according to the worst-case scenarios specified in the standards to evaluate the success of the designed filter.

In this study, the worst-case scenario suggested by the relevant standard has been taken into consideration, and the noise attenuations of the filter at different source/load impedances have been examined. Results are given in Section IV.

The EMI filter input to be designed in this study is connected to a high voltage DC source (DC-DC converter), and this connection point has a large C-valued capacitor against DC voltage fluctuations. In other words, the input of the EMI filter is low impedance due to this capacitor. Similarly, there is a low impedance network at the filter output (power grid). In this case, as the EMI filter has low impedance at both ends, the T-filter (LCL filter) has been chosen for the filter topology. Insertion loss (IL) calculation for T filter is given in (9).

$$IL_T = 20\log\left(\frac{V_o}{V_i}\right) = 20\log\left\{\frac{Z_S + Z_L + Z_{L1} + Z_{L2}}{Z_S + Z_L} + \frac{Z_S Z_L + Z_S Z_{L2} + Z_L Z_{L1}}{Z_C\,(Z_L + Z_S)} + \frac{Z_{L1} Z_{L2}}{Z_C}\right\} \quad (9)$$

In (9), Z_L and Z_S denote the load and source impedances, respectively. In measuring the noise suppression characteristics of EMC filtering devices, the load and source impedances are accepted as 0.1 Ω/100 Ω and 100 Ω/0.1 Ω for the situation called as worst-case scenarios according to the standard.

2) X AND Y CAPACITORS

EMI filter capacitors can be divided into two types: X capacitors (also known as line capacitors) and Y capacitors (line-to-ground capacitors). As DM noise is more dominant than CM noise in lower frequencies, capacitance values of X capacitors are higher than Y capacitors. However, selecting a high-value X capacitor causes the filter self-resonant frequency (SRF) to be low. Low SRF brings resonance problems and reduces the attenuation effect of the filter [29].

The connection of the X capacitors also influences filter attenuation. In X capacitors, directly connected between phases, resonance occurs at a higher frequency compared to the star-connected capacitors. This is because the equivalent series inductance (ESL) values of the two capacitors in the star connection are connected in series [30]. In the filter structure where the X capacitors are connected in star, the voltage levels are reduced. So, the capacitor cost is approximately 20% lower. Another reason for choosing star connection is to provide high power density.

The traditional capacitor selection approach in filter design is to choose metallized film or paper for X capacitors and ceramic disc type for Y capacitors. However, these two capacitors can be selected in different types by evaluating them in terms of stability, cost, and performance criteria.

Film capacitors can overcome dielectric breakdown with a small decrease in capacitance (C) value. This feature is called as self-healing. Metallized polypropylene (MP) film is preferred for the Y capacitor because of its better stability against time and temperature changes. Although usage of the ceramic disc for the Y capacitor is cost-effective, its lack of self-healing capability after voltage spike poses a major problem in terms of safety and reliability. Besides, the ceramic capacitor has a relatively low C value compared to the film capacitor. Thanks to their self-healing feature, MP capacitors are open circuits in case of failure. On the other hand, ceramic capacitors do not have this feature, and they are disadvantageous due to their short circuit nature. They also pose a risk of electric shock when losing ground connection [31].

3) COMMON MODE CHOKE

Since Y capacitors are used in the ground connection of the circuit, they are produced at limited C values due to the safety regulations. CM choke (CMC) is a special inductor designed for EMI filters. It has an important place in attenuating CM

noise due to the limited C value of the Y capacitor. Therefore, there are many studies on the modeling and design of the choke in the literature [32]–[34].

In three-phase systems, three winding CMC is commonly used. Since the currents are not always balanced in three-phase systems, the current flows from the neutral winding. When a winding for the neutral is added to the CMC, the magnetic fields created by the unbalanced currents will cancel each other. By this means, CMC becomes balanced. With this fourth winding, the saturation situation in the CMC core caused by unbalanced currents will also be prevented. The neutral winding in CMC is a design approach that contributes greatly to the power density, especially in high power applications. In addition to saturation prevention in the CMC core, the neutral winding in the CMC is also used to control each phase of the inverter separately in case of single-phase operation [35].

It is assumed that an ideal CMC affects CM noise only. However, this assumption is not exactly correct because of the leakage inductance between CMC's two windings. Since DM currents move in the opposite direction in the windings of an ideal CMC, the magnetic flux formed in the core is eliminated. Therefore, it is assumed that DM inductance is not present. However, lack of full coupling between windings causes leakage inductance. All the flux produced by a winding does not couple to the other winding. Therefore, some of the leakage flux does not disappear while DM currents flow through the windings. This leakage flux leads the windings to have a small DM inductance.

In EMI filters, leakage inductance has both affirmative and adverse impacts on the filter. DM inductance, which is a result of leakage inductance, is connected in series to each winding of CMC. Excessive leakage inductance may cause saturation of CMC at low AC current values. If the CMC is designed at a certain leakage inductance value, it is useful for filtering, and it does not have a saturation problem while carrying power line current. CMC is designed in a way that the leakage inductance value is between 0.5-5% of CM inductance according to the winding style [36].

One of the important design considerations for CMC is the winding style. There are two winding styles used for CMC. These are sectional and bifilar winding. Representation of the winding used in a single-phase application is given in Fig.6. The difference between these winding styles is the percentage of the leakage inductance. In sectional winding, leakage inductance is higher than bifilar winding. Also, voltage insulation is higher due to its separate winding.

Wounding wires together increases coupling and reduces DM impedance. Thus, DM attenuation of CMC is lower in bifilar winding than sectional winding. In the bifilar winding, there is low attenuation at the low-frequency range.

In this paper, as four wires (three-phase and neutral conductors) are twisted together, it is called multifilar winding. All wires of multifilar choke are insulated wires with different colors for safety.

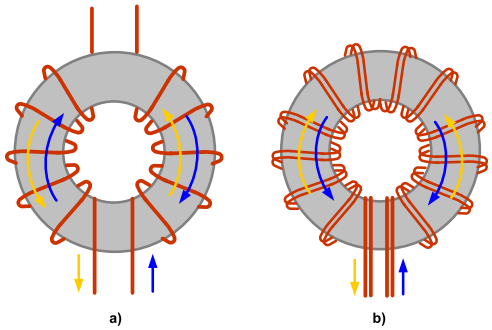


FIGURE 6. Different winding styles for CMC a) sectional winding b) bifilar winding.

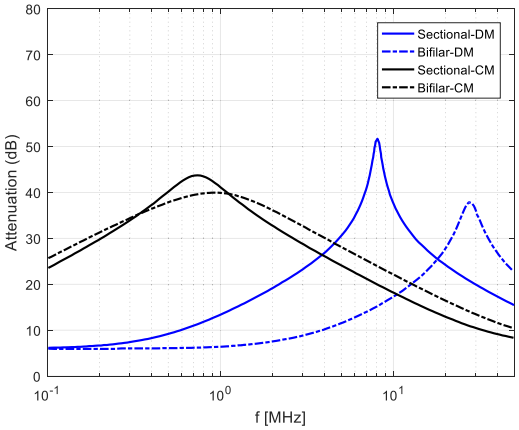


FIGURE 7. CM and DM insertion loss for sectional and bifilar winding chokes.

The effect of different windings on the CM and DM noise attenuation is given in Fig.7. It is seen that DM attenuation of bifilar winding is lower than sectional winding. CM attenuations of two windings are almost the same (the maximum difference is 4 dB).

If the coupling between two windings is high, then DM inductance is small. The windings of sectional winding CMC are not close to each other compared to the bifilar winding CMC. Thus, this results in high leakage inductance in the CMC. As the DM inductance is approximate between 0.5-5% of CM inductance, DM impedance will be smaller than CM impedance in low frequencies, as seen in Fig.7. The self-resonance frequency of the DM inductor of CMC is also higher than the CM inductor.

The formulas used for the inductance calculation of CMC (Fig.8) are given in (10) and (11).

The inductance of a coil wound on a toroid of permeable material is calculated in two parts [32]. Firstly, the inductance of an air-core toroid is calculated as in (10), and then it is multiplied by the effective permeability of one half of the toroid modeled as a rod core. Leakage inductance [33] is calculated as in (11), and expansion of l_{eff} is given in (12).

$$L = \frac{0.4\pi N^2 A_e}{l_e} \times 10^{-8} H \tag{10}$$

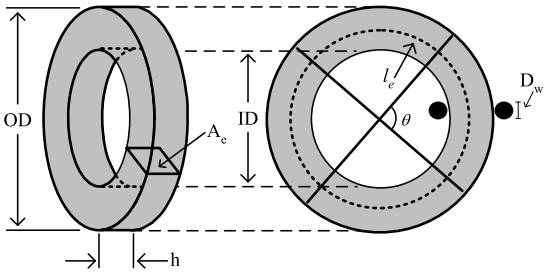


FIGURE 8. Calculation of CMC inductance.

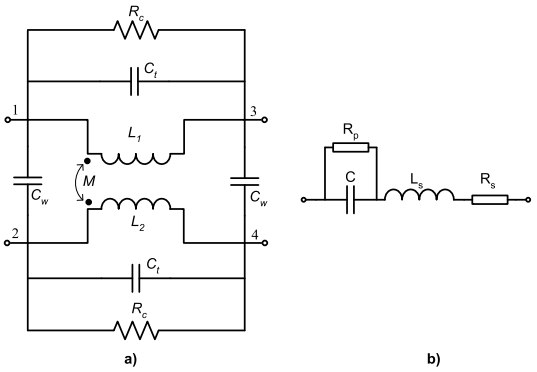


FIGURE 9. Equivalent circuits for (a) CMC and (b) capacitor.

$$L_{DM} \cong 2.5\mu_0 N^2 \frac{A_e}{l_{eff}} \left(\frac{l_e}{2}\sqrt{\frac{\pi}{A_e}}\right)^{1.45} \tag{11}$$

$$l_{eff} = \sqrt{\frac{OD^2}{\sqrt{2}}\left(\frac{\theta}{4}+1+\sin\frac{\theta}{2}\right)^2 + ID^2\left(\frac{\theta}{4}-1+\sin\frac{\theta}{2}\right)^2} \tag{12}$$

Definitions of abbreviations are given below.

A_e: cross-section of the core

l_e: the mean path length of the toroid core (from manufacturer's datasheet)

l_{eff}: the effective mean path length of leakage flux

D_w: diameter of the wire

OD and *ID* are outer and internal diameters of the toroid core.

To build an accurate model, high-frequency equivalent circuits of the filter elements are required. Equivalent circuits of CMC and capacitor, which are used in the study, are given in Fig.9.

C_t, C_w, R_C, M are parasitic self-capacitance, the capacitance between winding, resistance for magnetic losses, and the coupling factor of CMC, respectively. For the capacitor model, R_p, R_s, L_s are leakage resistance, equivalent series resistance (ESR), and equivalent series inductance (ESL).

B. LEAKAGE CURRENT CALCULATION FOR EMI FILTER

In the filter design, a low impedance path for high-frequency noise is created with a Y capacitor which is connected between phase/neutral lines and ground. In this way, EMI is reduced. Although Y capacitors with large capacitance values reduce EMI, high capacitance values cause an increase in ground leakage current. The ground leakage current flows through the protective ground conductor or device body (chassis). In cases where there is no ground connection, or this connection is lost, the current can flow through the human body. This leakage current has been limited in many applications by international safety organizations (EN 60950-1 for information technology devices, IEC60601 for medical equipment, EN 55014 for devices used in homes and similar places) to prevent danger to human life.

If the inverter is evaluated as a Class I device according to IEC 60950, the maximum leakage current value at 50 Hz should be 3.5 mA. Accordingly, the maximum C_Y capacitance value that will ensure the leakage current limit according to the upper limit of the grid voltage RMS value is calculated with (13).

$$C_{Y,\max} = \frac{I_{leakage,\max}}{1.1 \times V_g \times 2\pi f_g} \tag{13}$$

From (13), the maximum value of C_Y is obtained as 44.035 nF. Since Y capacitors are connected between phase conductors and ground, high capacitance values cause a high leakage current in case of a possible fault. Therefore, this current can damage any living species upon touching the body of the device. Therefore, touch current, which is crucial for safety, must be considered in filter design.

The maximum value that the C_Y capacitor can take is determined via the touch current. The standard that determines this current value is EN60335-1 in this study. The touch current value regulated by the standard for Class I devices is 3.5 mA [8]. Calculation of the touch current is given as follows:

$$\begin{aligned} I_{touch} &= I_{C_{CM}} + I_{C_{bus}} \\ I_{C_{CM}(\max)} &= 2\pi f_L C_{CM} V_{g(\max)} \\ I_{C_{bus}} &= 2 \times 2\pi f_L \times 2C_{bus} V_{CM(\max)} \end{aligned} \tag{14}$$

In (14), C_{bus}, $V_{g(max)}$, and $V_{CM(max)}$ define the bus bar capacitance, maximum network voltage, and maximum CM voltage, respectively.

As limiting the leakage current is an important safety issue, in this regard, the standard that grid-connected PV systems must comply with the German VDE 0126-1-1 standard, which specifies the maximum allowable leakage current. RMS value of the ground leakage current in filter design for PV systems is limited to 300 mA.

Another standard in EMI filter design regarding the leakage current for three-phase filters is EN60939 standard. This standard includes leakage current information, measurement, and calculation procedures for industrial filters within the enclosure. Considering that the star points of the load and the source are connected over a Z impedance in three-phase systems, a voltage drop on this Z impedance occurs due to the leakage current. In three-phase balanced systems, the sum of currents is zero, and no current will flow from the star point. However, it is not possible to claim an existing balanced

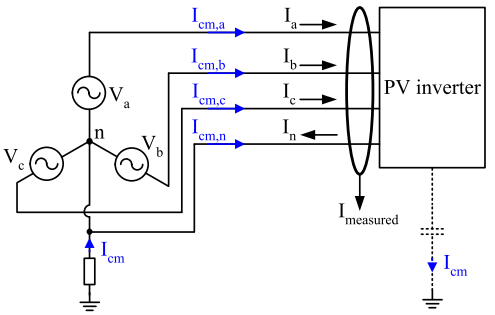


FIGURE 10. Leakage current measurement for three-phase four-wire systems [37].

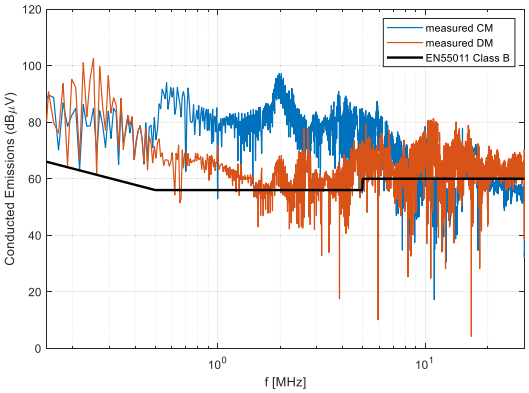


FIGURE 11. CM and DM noise results without the filter.

system because of the voltage unbalance in the network and the tolerances of the filter capacitors. The determining factor of the leakage current is the voltage drop caused by the unbalance of the X capacitors connected between the phases.

Though the rated values of the capacitors are identical in most filters, the values may vary depending on the manufacturing tolerance. Tolerances of the commercially available ceramic and film capacitor change between 0.1% and 20%. Accordingly, for the Y capacitor to be selected, the leakage current is calculated, and the maximum capacitance value is determined. The largest voltage drop on C_Y will occur if one of the X capacitors shows the highest tolerance value and the others show the lowest tolerance value.

The leakage current calculation is obtained based on the assumption that the grid voltage unbalance is 3%, as specified in the EN50160 standard. So, the leakage current calculation for the designed filter is calculated by considering that filter as a separate industrial 400V three-phase filter. According to the manufacturer datasheet, the tolerance value of the capacitors used in the filter design is selected as ± 20% of the rated value. For example, in this study, the values of X and Y capacitors are selected as 0.68μ F and 4.7 nF, respectively. Thereby, if the EMI filter is considered separately, the calculated leakage current value of the EMI filter becomes 66.75 μA.

As a result, since the element limiting the leakage current to the ground is the Y capacitor, a smaller value of this capacitor will give a lower leakage current. In order to measure the leakage current, a measurement setup for three-phase, four-wire systems is given in Fig.10.

For the leakage current measurement, a current probe is connected around the three-phase and neutral conductors. The current read at the current probe is calculated as in (15).

$$\begin{aligned} I_{measured} &= \left(I_a + I_{cm,a}\right) + \left(I_b + I_{cm,b}\right) + \left(I_c + I_{cm,c}\right) \\ &\quad + \left(-I_n + I_{cm,n}\right) \\ &= \left(I_a + I_b + I_c - I_n\right) + \left(I_{cm,a} + I_{cm,b} + I_{cm,c} + I_{cm,n}\right) \end{aligned} \tag{15}$$

In three-phase four-wire systems, since the sum of phase currents and neutral current is zero, the measured current value is calculated as in (16).

$$I_{measured} = I_{cm} = I_{cm,a} + I_{cm,b} + I_{cm,c} + I_{cm,n} \tag{16}$$

As the inverter circuit is transformerless and does not have galvanic isolation, the leakage current becomes an important issue. Although transformerless PV inverters have higher efficiency than isolated alternatives, large leakage current may flow through a conductive connection between the parasitic capacitance of the PV panels and the ground. The leakage current seen in PV systems affects the power quality, safety concerns, as well as electromagnetic compatibility. In addition to that, it decreases the lifespan of PV modules [38].

C. EMI FILTER DESIGN STEPS

EMI filter design procedure is given in this section. In the filter design process, filter topology and impedance mismatch issues are also considered. Design steps are as follows:

Step 1: CM and DM noises, as seen in Fig.11, are measured. Fig.11 shows these two noise modes obtained from the noise measurements of phase A and the neutral line.

Step 2: With (17) and (18), CM attenuation requirement ($V_{req,CM}$) and DM attenuation requirement ($V_{req,DM}$) are calculated. The drawing of required attenuations in a logarithmic scale is given in Fig.12.

$$V_{required,CM}\,[dB\mu V] = measuredV_{CM} - SL + SM \tag{17}$$

$$V_{required,CM}\,[dB\mu V] = measuredV_{CM} - SL + SM \tag{18}$$

In the equations, *SL* and *SM* are the standard limits and the safety margin. As in many filter design applications, the safety margin is determined as 6 dB in this study.

Step 3: Suppression of a frequency range can simply be determined via the required noise attenuation calculation. Additionally, the required noise attenuation is used for specifying the filter topology. As the maximum value of the required noise is greater than 40 dBμV, a three-element filter design is necessary. LCL filter topology is chosen according to the impedance mismatch described in the previous section. The corner frequency of the EMI filter can be found by drawing a 40 dB/decade slope line tangent to required CM and DM noise attenuations. When the graphical method [9]

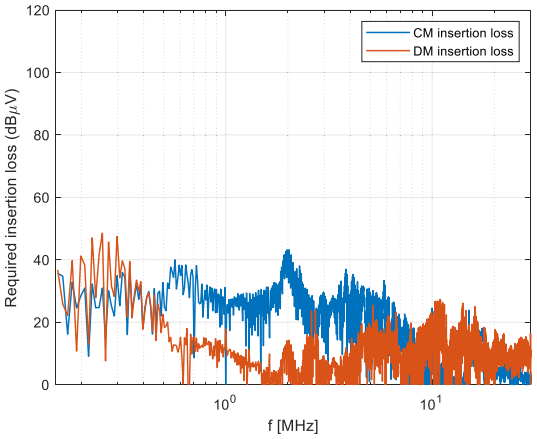


FIGURE 12. Required CM and DM attenuation.

is used to specify the corner frequency, the corner frequencies are found as $f_{c,CM} = 66.8$ kHz for CM and $f_{c,DM} = 82.9$ kHz for DM noise.

Step 4: Firstly, the CM filter and its circuit elements will be specified in this step. The Y capacitor value is the main determining factor for the CM EMI filter design. According to the 3.5 mA maximum touch current constraint (specified by the EN60335-1 standard), the largest value of the Y capacitor is calculated as 20.174 nF in equation (13). KEMET's 4.7 nF Y2 capacitor is chosen as the C_Y capacitor that meets the maximum allowance of ground leakage current requirement specified in the German standard VDE V 0126–1–1. This C_Y ensures the maximum allowance of touch current requirement of EN60335-1. In this study, the leakage current is calculated considering the capacitor tolerance values, and it was observed that the touch current determined by the relevant standards is also provided. Simulation and experimental measurement of ground leakage current will be made according to the selected Y2 capacitor.

For the CM filter stage, CM inductance is calculated by using (19).

$$f_{c,CM} = \frac{1}{2\pi\sqrt{2L_{CM}C_{DM}}} \rightarrow L_{CM} = 1\Big/\left(8\pi^2 f_{c,CM}^2 C_{CM}\right) \quad (19)$$

Calculated CM inductance from (19) is $L_{CM} = 603.89\ \mu$H. Two CMCs with different winding styles are used to obtain this inductance value. CMC 1 is designed with sectional winding, and it has six turns. CMC 2 is designed with multifilar winding, and it has seven turns. Mn-Zn toroid core of Cosmo T63 series is used for the CMC core. From the datasheet of the toroidal core [39], $\mu_r = 3000$ (material CF130), $l_e = 152.1$ mm, $A_e = 244.7\text{mm}^2$, and these values are used for the inductance calculation. When subtended angle (θ) of winding on the core is approximately 70 degrees for CMC 1 (sectional winding), $L_{CM} = 603.5\ \mu$H and $L_{DM} = 5.12\ \mu$H are obtained as a result of the inductance calculations according to (10-12). These values are calculated for CMC 2 (multifilar winding) as 605.1 μH and 1.72 μH, respectively. The inductances for both CMCs are measured by LCR meter, and the measured inductance values are given below.

CMC 1: $L_{CM} = 614.47\ \mu$H, $L_{DM} = 5.46\ \mu$H (measured @10 kHz), $L_{DM} = 0.89\%$ of L_{CM}

CMC 2: $L_{CM} = 614.04\ \mu$H, $L_{DM} = 1.97\ \mu$H (measured @10 kHz), $L_{DM} = 0.33\%$ of L_{CM}

As a result, the design of the CM filter stage is completed. Then, the DM filter design will be made.

Step 5: Although CMC is a crucial component of the CM filter, it can also attenuate some DM noise by its leakage inductance. As a result of the measurement, it is seen that the CMC leakage inductances are changing within the 0.3-0.9% range of the rated inductance according to the winding style. Although the stray inductance is often undesirable in the filter design, the use of this inductance as DM inductance creates an advantageous situation.

A similar calculation is obtained for the DM filter stage. DM filter corner frequency is 82.9 kHz, and measured leakage inductance of CMC is used as DM inductance (5.46 μH). Finally, the DM capacitor is calculated as below (20).

$$f_{c,DM} = \frac{1}{2\pi\sqrt{0.5L_{DM}C_{DM}}} \rightarrow C_{DM} = 0.5C_X = 1\Big/\left(8\pi^2 f_{c,DM}^2 L_{DM}\right) \quad (20)$$

DM capacitor is calculated as $C_{X(1)} = 0.675\ \mu$F and $C_{X(2)} = 0.935\ \mu$F for LCL filter 1 and LCL filter 2, respectively. Using CMC leakage inductance as a DM inductor aims to increase the power density by making a filter design so that no inductor is needed for DM noise. Since there are two CMCs in the T-type EMI filter, the leakage inductance for DM noise will be two times higher, which will contribute to the attenuation of the DM noise without the need for an extra inductor. A more efficient filter design is achieved via this approach, which leads to a reduction in both the cost and volume of the circuit.

Only X capacitors are used for DM noise in the filter design. X capacitors are sufficient in attenuating DM noise because the leakage inductance value occurring between the windings of the CMC has a sufficient effect on the DM noise. Thus, a better design has been achieved in terms of power density.

The filter design is obtained for both modes according to the calculation given above. Finally, components of the filter are $L_{CM1} = 614.47\ \mu$H ($L_{leakage1} = 5.46\ \mu$H), $L_{CM2} = 614.04\ \mu$H ($L_{leakage2} = 1.97\ \mu$H), $C_{Y2} = 4.7$ nF, $C_{X2(1)} = 0.680\ \mu$F and $C_{X2(2)} = 1\ \mu$F.

It has been observed that the difference of the measured noise without a filter from the standard limit value is more than 40 dB. Therefore, when the parasitic effects of the filter elements are also considered, the two-element filter (i.e., LC or CL filter) design will not be sufficient in suppressing the noise. Instead, three-element filter topologies (T or π) should be preferred. These two topologies are used according to the input and output impedance state. In the T filter, input

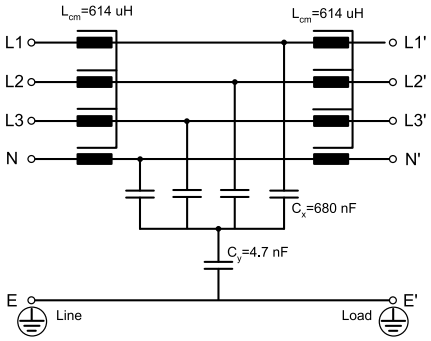


FIGURE 13. LCL (T) filter topology.

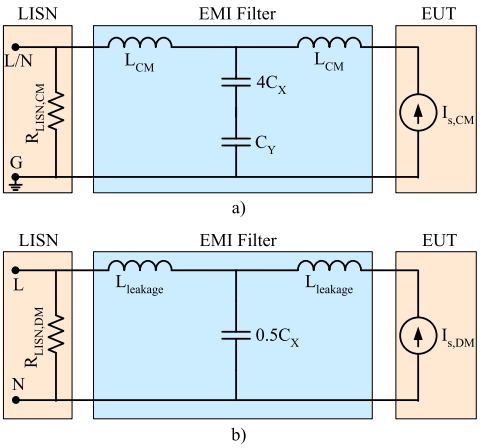


FIGURE 14. Equivalent circuit of designed EMI filter a) common mode b) differential mode.

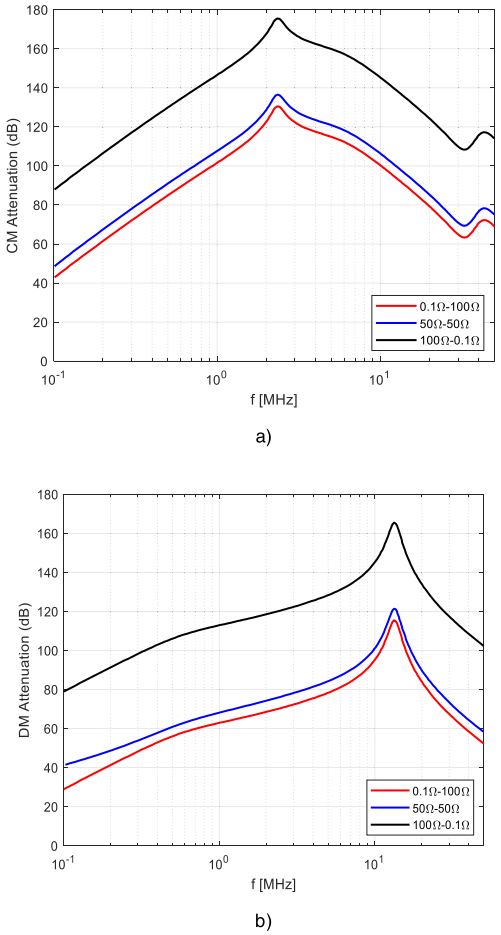


FIGURE 15. Filter noise attenuation under different source and load conditions a) CM b) DM.

and output impedances are high, while in the π filter they are low.

According to the noise modes, the proposed filter topology and equivalent circuits are given in Fig.13 and Fig.14, respectively.

In the filter design carried out in this study, instead of using a Y capacitor in the connection of each phase to the ground, a single Y capacitor is connected to the artificial star point formed by the X capacitors. A cost-effective design has been made using fewer Y capacitors with this layout. The ground leakage current has been reduced by limiting the Y capacitor value, and the power density has been improved with a design that takes up less space.

A study has observed that the direct connection of X and Y capacitors to conductors gives better results than wye-connected capacitors (about 5 dB in CM noise) [30]. However, the use of more than one Y capacitor for the ground connection of each conductor in direct connection increases the cost and size of the filter.

The filter topologies used in the study are summarized in Table 2.

The effect of different impedance values on T-filter attenuation is seen in Fig.15 by simulating filter insertion loss for CM and DM. Impedance cases shown in Fig.15 are Case 1: $Z_S = 50\ \Omega$-$Z_L = 50\ \Omega$, Case 2: $Z_S = 0.1\ \Omega$-$Z_L = 100\ \Omega$ and Case 3: $Z_S = 100\ \Omega$-$Z_L = 0.1\ \Omega$. The simulation study of the filter is carried out via the LTspice software program using these impedances. The best attenuation for both CM and DM noise is Case 3, and the worst attenuation is Case 2.

TABLE 2. Summary table of the EMI filter topologies.

Filter type	Value of filter elements		
LCL filter 1	L_{CM}=614.47 µH ($L_{leakage}$=5.46 µH)	C_{X2}=0.680 µF	C_{Y2}=4.7 nF
LCL filter 2	L_{CM}=614.04 µH ($L_{leakage}$=1.97 µH)	C_{X2}=1 µF	C_{Y2}=4.7 nF
CLC filter	L_{CM}=614.47 µH ($L_{leakage}$=5.46 µH)	C_{X2}=0.680 µF	C_{Y2}=4.7 nF

To sum up, the advantages of the proposed filter structure are given below.

- A smaller leakage current has been obtained since a single Y capacitor is used.

- Four-winding choke is used to prevent CMC core saturation caused by the current flowing from the neutral in the case of a voltage unbalance.

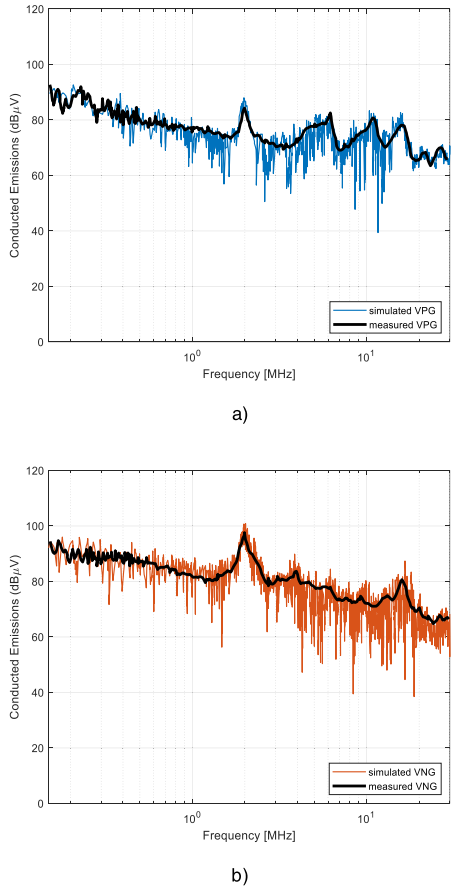


FIGURE 16. Total conducted emissions obtained from simulation and receiver (without the EMI filter) a) line-to-ground b) neutral-to-ground.

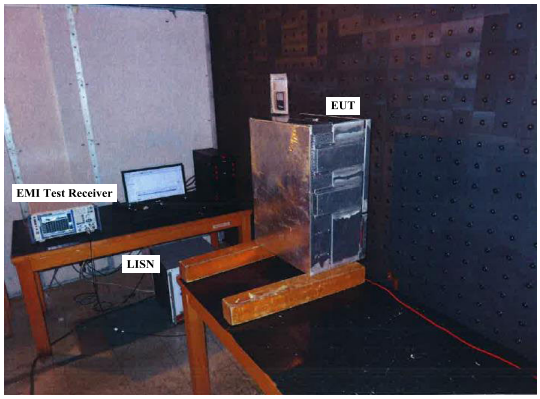


FIGURE 17. Experimental measurement test bench in an anechoic chamber.

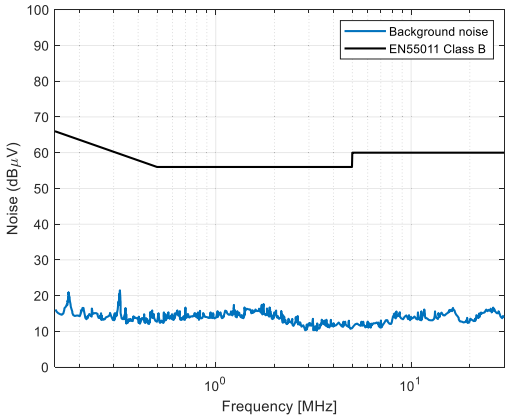


FIGURE 18. The background noise of the test room.

- Low volumetric design is achieved with the use of leakage inductance as the DM inductor.

IV. EXPERIMENTAL AND SIMULATION RESULTS

Simulation and experimental studies are conducted to validate this novel inverter modeling. The simulation model of the inverter is built in MATLAB/Simulink environment to verify the modeled inverter circuit. Fig.16 gives the comparison of simulated and measured CE voltage of line and neutral conductors. The difference between the simulation model and experimentally measured spectra is approximately 8 dBμV. According to the EMC measurement given in Fig.16, measured and calculated results match each other well.

According to the EN55011 standard, the arrangement of the equipment is given in Fig.17. The LISN used in the experimental study is CISPR 16-1-2/ANSI C63.4 compliant equipment of Rohde&Schwarz company. The EMI receiver used in the measurements is the R&S ESU model of Rohde&Schwarz. Peak (PK) detector is used in the measurement with the EMI receiver. The measurement repetition with the quasi-peak (QP) detector is not required as the measurement values of the QP detector are smaller than the PK detector.

The limit lines for the EN55011 EMC standard, of which the PV inverter must comply with, are given in Fig.11. Since the inverter can also be used for single-phase applications, the filter has been designed according to Class B EMC requirement limits.

To compare the measurements taken in the laboratory and provide a more reliable measurement setup, the background noise (called as ambient noise) is also measured. The background noise is taken when the power cord is not connected to EMC measurement devices, and the level of this noise is approximately 15 dBμV, as seen in Fig.18.

Although background noise is mostly considered in radiated emission measurements, it is also considered for conducted emission measurement in this study. As the measured background noise is at very low levels, it is observed that there is no problem regarding measurement accuracy.

Measurement uncertainty is also another important issue in EMC testing. Uncertainty affects the outcome of the EMC test, and it is useful for the statement of pass/failure. Measurement uncertainties and levels of uncertainties are defined in the CISPR-16-4-2 [40] for conducted disturbance (mains port). Value of standard measurement uncertainty U_{CISPR} is 3.6 dB for the frequency range of 0.15 kHz to 30 MHz. So, a test laboratory's measurement uncertainty (U_{lab}) must be smaller than standard measurement uncertainty U_{CISPR}. In this study, U_{lab} is calculated as 2.9 dB based on uncertainty contributors (spectrum analyzer and LISN).

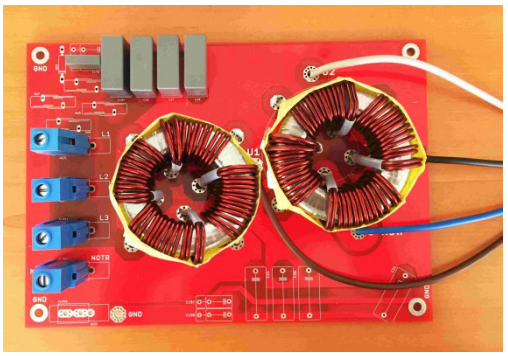


FIGURE 19. Designed EMI filter 1 for PV inverter.

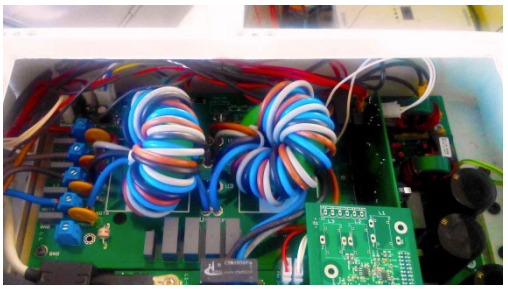


FIGURE 20. Designed EMI filter 2 for PV inverter.

Finally, the EMI filters obtained from the filter design steps are given in Fig.19 and Fig.20.

Fig.19 shows sectional winding CMC, while Fig.20 shows multifilar winding CMC.

The EMI filter board's dimensions in Fig.19 are 205 mm×145 mm×40 mm. Therefore, the designed filter has a boxed volume of 1189 cm^3 (72.56 in^3), and the power density of the filter is 344.54 W/in^3 (21.03 kW/dm^3). The proposed filter design is better than the filter with 215 W/in^3 (13.1 kW/dm^3) power density given in [10].

Although the main focus of this paper is on conducted emission interference, it is seen that adding C_Y capacitors (as seen in Fig.20) between phase/neutral lines and ground has a small (∼3 dB) CM noise reduction above 25 MHz. The effect of this configuration has precisely seen in the RE test of the inverter.

In the filter design shown in Fig.19 and Fig.20, the capacitor pin connections are kept as short as possible since it is important to increase the capacitor SRF.

The importance of the filter arrangement has been explained in previous sections. In this section, to give an example for the situation where impedance mismatch is not considered, a π-filter (CLC filter) is designed by using filter elements of the same value. In this case, it is seen that the filter does not meet the expected frequency region, which is nearly up to 1.5 MHz, and is insufficient in suppressing the noise. Noise suppression effectiveness of these different EMI filter topologies is given in Fig.21 (Filter-1: T filter and Filter-2: π-filter). It has been observed that the interference increases by choosing a capacitor instead of an inductor as the element facing the noise source side of the filter.

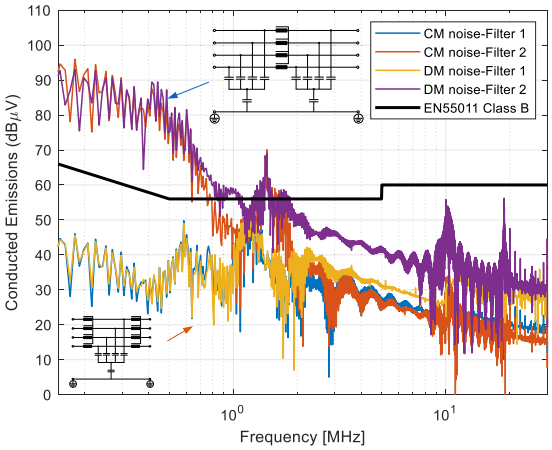


FIGURE 21. Comparison of different filter topologies according to the impedance mismatch (Filter 1-LCL and Filter 2-CLC).

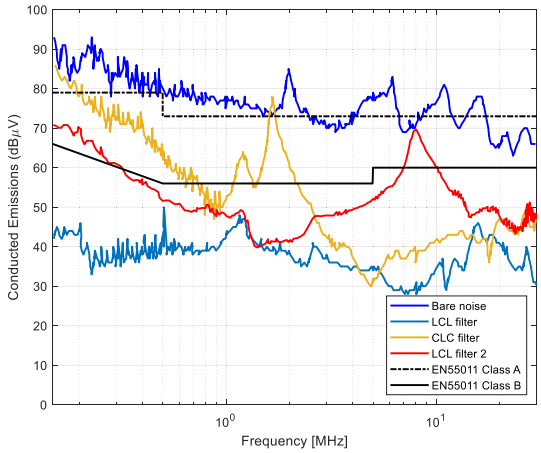
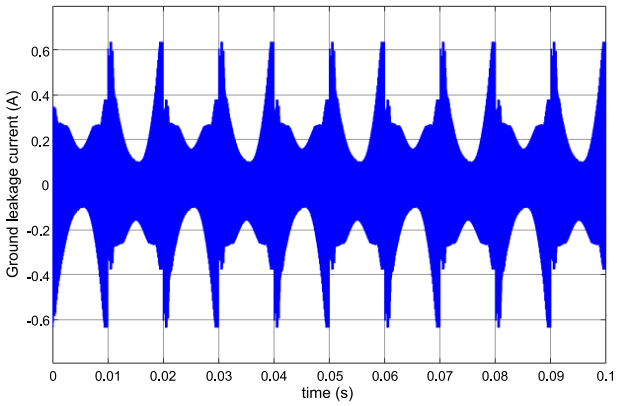


FIGURE 22. EMC measurement results for line A in the 150 kHz-30 MHz frequency range.

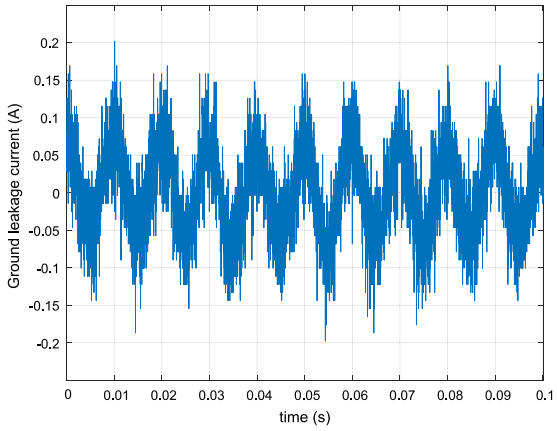
According to the results in Fig.21, the π filter does not give good attenuation between 0.15-1.5 MHz compared to the T filter.

Laboratory measurement results of phase A for both designed filters are also given in Fig.22. The conducted emission noise voltage is lower than the standard limits for filter 1 (LCL filter with sectional winding CMC). According to Class B limits, other filter designs are not adequate to suppress the EMI noise. As it can be seen in Fig.22, the π-filter remains above the standard limits at low frequencies whose measurements were obtained via the PK detector. On the other hand, filter 2 (LCL filter with multifilar winding CMC) can ensure the Class A limit, which is higher than Class B.

EMC measurements show that LCL filter with sectional winding CMC ensures the standard limits. As the final step of the filter design, ground leakage current measurement is conducted to satisfy safety regulations. Figures of the ground leakage current obtained from the simulation and experimental studies are given in Fig.23(a) and Fig.23(b), respectively. The leakage capacitance to the ground is responsible for ground leakage current and varies with the surface of PV panels. The leakage capacitance is found to be 50 − 150nF/kW



a)



b)

FIGURE 23. Ground leakage current a) simulation b) experimental.

for glass-faced PV modules and up to 1uF/kW for thin-film PV modules [41]. In the simulation, the parasitic capacitance to the ground is chosen 140 nF as in [12].

According to the simulation results, the RMS value of the leakage current is 64.012 mA, while the ground leakage current value is measured as 60 mA in the experimental study. In the study, the difference between the experimental and simulation studies is seen in the ground current's peak values. In the leakage current calculation for a solar inverter with long cables and variable parasitic capacitance, a realistic estimation of the current is not easy. However, RMS values of simulated and experimental results are very close to each other. For the PV inverters, according to section 7.10.2 of the NB32004-2018 directive, the ground leakage current limit value is 300 mA for inverters with a rated output power of 30 kVA and below while this value is 10mA/kVA at powers above 30 kVA. As the PV inverter used in this study is 25 kVA, it ensures the ground leakage current (300 mA) limit according to VDE 0126-1-1 and NB32004-2018 recommendations.

V. CONCLUSION

EMI filter design is challenging for power electronics applications, especially inverters. Since the design of a filter is peculiar to the circuit, noise modeling of the circuit should be created. This paper proposes a novel design of an EMI filter for a three-level, three-phase, four-wire grid-connected PV inverter. A simulation study has been conducted to verify the success of the designed EMI filter, and all findings are experimentally confirmed that the standard limits have been met. The simulation and experimental results validate the performance of the filter.

In the study, two different winding styles are used for CMC, and the effect of the windings is compared. In addition to CMC's winding style, the importance of the impedance mismatch for EMI filter design is also examined. The results obtained from this study could be a guide for the designers.

The leakage inductance of CMC is used as a DM inductor to avoid bulky filter design. The leakage inductance effect, which is an undesirable effect for CMC, has become advantageous, and the use of extra elements is no longer needed in terms of power density. Also, the filter design with a single Y-capacitor has improved the power density of the inverter. EMI noise and ground leakage current are restricted to specific levels according to the recommendation of international standards and regulations. With this study, technical experience on a filter design is shared.

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