



Research Article

MODELING OF THREE-PHASE THREE-LEVEL RECTIFIER WITH SPACE VECTOR PULSE WIDTH MODULATION METHOD IN MATLAB/SIMULINK PROGRAM

Halil İbrahim YÜKSEK*¹, Uğur ARİFOĞLU²

¹*Gümüşhane University, Department of Electrical and Electronics Engineering, GÜMÜŞHANE;*
ORCID: 0000-0001-8740-6596

²*Sakarya University, Dept. of Electrical and Electronics Eng., SAKARYA; ORCID: 0000-0001-8082-5448*

Received: 22.06.2019 Revised: 22.10.2019 Accepted: 17.12.2019

ABSTRACT

Multi-level rectifiers have low harmonic content and electromagnetic interference (EMI). In recent years, especially in medium and high-power applications are increasing use. As the voltage level per switch and switching frequency are low, the multi-level rectifiers have low losses and high efficiency. In this study, three-level neutral point clamped (NPC) rectifier topology with pulse width modulation (PWM) is investigated and the decoupled equations in the d-q synchronous rotating axis of the rectifier are given and a space vector PWM (SVPWM) control algorithm based on the d-q synchronous rotating axis of three-level rectifier is proposed. The control of the whole system is provided by voltage oriented control (VOC) strategy, which enables the realization of control in cascade system with outer voltage and inner current control blocks. This paper is focused on explaining in detail modulus optimum and symmetrical optimum methods used in the design of the inner current and outer voltage PI controllers of the three-level rectifiers, respectively. PI voltage controller is used to keep the rectifier output voltage constant, and PI current controller is used to reduce the harmonic content of the grid current. In addition, a simplified method compared to conventional SVPWM is used to calculate switching times and switching sequences. In this study, three-level rectifier is simulated in Matlab / Simulink with the help of SVPWM. The performance of the circuit has been tested by changing both the load value and the load voltage suddenly and successful results have been achieved.

Keywords: Three-level rectifier, space vector pulse width modulation, voltage oriented control, modulus optimum, symmetrical optimum.

1. INTRODUCTION

Rectifiers with diodes (uncontrolled) are commonly used in alternating current (AC)/direct current (DC) power conversion. As the total harmonic distortion (THD) value of the currents is high, the diode rectifiers are replaced by controlled rectifiers that are grid friendly. The pulse width modulated (PWM) rectifier is also superior to the diode rectifier because of its features such as low harmonic grid current, bidirectional power flow, adjustable output voltage and high power factor.

* Corresponding Author: e-mail: halilibrahimyukse05@gmail.com, tel: (456) 233 10 00 / 1655

Harmonics injected in to the grid by rectifiers both damage the grid-connected loads (overvoltage, overheating, etc.) and lead to inefficient operation [1]. Uncontrolled rectifier circuits containing passive harmonic filters to eliminate the harmonics they produce are replaced by controlled rectifier circuits using semiconductor elements such as GTO and IGBT.

The voltage sourced rectifier (VSR) which know as an boost type rectifier is preferred because of the advantages such as low THD of input current, bidirectional power flow [2] and high power factor [3-5]. Multi-level rectifiers are increasingly used in medium and high power applications due to decreasing harmonic content [6], low electromagnetic interference (EMI) value and high efficiency. Since both the voltage per switch and the switching frequency in multi-level rectifiers are low, the losses are low in this circuits and their efficiency is high. Due to the above mentioned advantages, performance of three-level neutral point clamped PWM rectifier is high compared to two-level PWM rectifier in medium and high power applications [7].

There are many different PWM techniques for controlling of multi-level rectifiers such as sinusoidal PWM (SPWM), harmonic elimination PWM, minimum current ripple PWM, third harmonic injection PWM, modified sinusoidal PWM and sigma delta modulation technique [8-11]. SPWM technique is widely used in rectifier circuits but this technique is inefficient due to high switching frequency [7]. High switching frequency cause to increased switching losses and high ripple in output voltage. A space vector PWM (SVPWM) method was developed for reducing these negative aspects [12]. As it decreases both the THD value of the grid current and the ripple of the DC output voltage according to the SPWM, the use of this method is increasing nowadays.

In this paper, simulation model of three-level rectifier controlled by SVPWM is created. The simplified method compared to conventional SVPWM is used to calculate switching times and switching sequences. The control of the whole system is provided by VOC strategy, which enables the realization of control in cascade system with outer voltage and inner current control blocks. In the outer voltage controller design, the symmetrical optimum method is preferred to eliminate time delays and optimize disturbance of input. In the inner current controller design, the modulus optimum method is preferred because of the structure of the system transfer function as well as providing fast response and simplicity.

2. MATHEMATICAL MODEL

A three-level VSR circuit diagram is shown in Figure 1 [13]. In this circuit, R_s and L_s are the resistance and inductance values between power supply and rectifier, respectively. S_{ni} ($n = 1, 2, 3, 4$ and $i = a, b, c$) represent the 12 different switching states of the rectifier. C_{dc1} and C_{dc2} are the capacitors for the DC side. e_i and i_i are the voltages and currents of three-phase grid, respectively and v_i are the voltage values for the AC side of the rectifier. V_{dc1} and V_{dc2} are the voltage values of C_{dc1} and C_{dc2} for the DC side, respectively. i_0 is the current flowing from neutral point. AC voltage feeding the NPC rectifier is three-phase, balanced and the grid has not neutral point. The input voltage of NPC rectifier is given in equation (1).

$$\begin{cases} e_a = V_m \cdot \sin(\omega t) \\ e_b = V_m \cdot \sin\left(\omega t - \frac{2\pi}{3}\right) \\ e_c = V_m \cdot \sin\left(\omega t + \frac{2\pi}{3}\right) \end{cases} \quad (1)$$

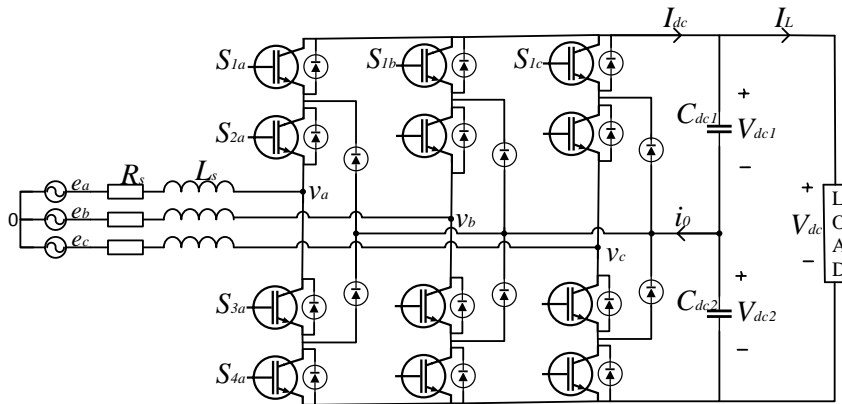


Figure 1. Circuit diagram of three-level VSR

In order to construct the mathematical model of the NPC rectifier with PWM, the Kirchoff voltage law is applied to the grid side as shown in equation (2) and the Kirchoff current law is applied to the load side as shown in equation (3).

$$\begin{cases} e_a = L_s \cdot \frac{di_a}{dt} + R_s \cdot i_a + (S_{ap} - S'_p)V_{dc1} + (S_{an} - S'_n)V_{dc2} \\ e_b = L_s \cdot \frac{di_b}{dt} + R_s \cdot i_b + (S_{bp} - S'_p)V_{dc1} + (S_{bn} - S'_n)V_{dc2} \\ e_c = L_s \cdot \frac{di_c}{dt} + R_s \cdot i_c + (S_{cp} - S'_p)V_{dc1} + (S_{cn} - S'_n)V_{dc2} \end{cases} \quad (2)$$

$$\begin{cases} S_{ap} \cdot i_a + S_{bp} \cdot i_b + S_{cp} \cdot i_c = I_L + C_{dc1} \cdot \frac{dV_{dc1}}{dt} \\ -S_{an} \cdot i_a - S_{bn} \cdot i_b - S_{cn} \cdot i_c = I_L + C_{dc2} \cdot \frac{dV_{dc2}}{dt} \end{cases} \quad (3)$$

S'_p and S'_n shown in equation (3) is given in equation (4).

$$S'_p = \frac{S_{ap} + S_{bp} + S_{cp}}{3}, S'_n = \frac{S_{an} + S_{bn} + S_{cn}}{3} \quad (4)$$

The state space equations for the mathematical model of the NPC rectifier given in equation (2)-(3) are shown in equation (5).

$$Z\dot{x} = Ax + Be$$

$$x = \begin{bmatrix} i_a \\ i_b \\ i_c \\ V_{dc1} \\ V_{dc2} \end{bmatrix}, e = \begin{bmatrix} e_a \\ e_b \\ e_c \\ I_L \\ I_L \end{bmatrix}$$

$$Z = [L_s \quad L_s \quad L_s \quad C_{dc1} \quad C_{dc2}] \tag{5}$$

$$A = \begin{bmatrix} -R_s & 0 & 0 & -(S_{ap} - S'_p) & (S_{an} - S'_n) \\ 0 & -R_s & 0 & -(S_{bp} - S'_p) & (S_{bn} - S'_n) \\ 0 & 0 & -R_s & -(S_{cp} - S'_p) & (S_{cn} - S'_n) \\ S_{ap} & S_{bp} & S_{cp} & 0 & 0 \\ -S_{an} & -S_{bn} & -S_{cn} & 0 & 0 \end{bmatrix}$$

$$B = [1 \quad 1 \quad 1 \quad -1 \quad -1]$$

According to the VOC strategy, the Park transformation given in equation (6) use to return from a-b-c stationary coordinates frame to d-q synchronous rotating reference frame [14].

$$f_{abc \rightarrow dq0} = \frac{2}{3} \cdot \begin{bmatrix} \cos \theta & \cos(\theta - \frac{2}{3}\pi) & \cos(\theta + \frac{2}{3}\pi) \\ -\sin \theta & -\sin(\theta - \frac{2}{3}\pi) & -\sin(\theta + \frac{2}{3}\pi) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{6}$$

The mathematical model in the d-q synchronous rotating axis obtained by using equation (6) is given in equation (7).

$$Z'\dot{x} = A'x + B'e$$

$$x = \begin{bmatrix} i_d \\ i_q \\ V_{dc1} \\ V_{dc2} \end{bmatrix}, e = \begin{bmatrix} e_d \\ e_q \\ I_L \\ I_L \end{bmatrix}$$

$$Z' = [L_s \quad L_s \quad C_{dc1} \quad C_{dc2}] \tag{7}$$

$$A' = \begin{bmatrix} -R_s & \omega L_s & -S_{dp} & S_{dn} \\ -\omega L_s & -R_s & -S_{qp} & S_{qn} \\ S_{dp} & S_{qp} & 0 & 0 \\ -S_{dn} & -S_{qn} & 0 & 0 \end{bmatrix}$$

$$B' = [1 \quad 1 \quad -1 \quad -1]$$

The vectors of grid voltage V_d and V_q in the AC side of the rectifier are given in equation (8).

$$\begin{cases} V_d = S_{dp} \cdot V_{dc1} - S_{dn} \cdot V_{dc2} \\ V_q = S_{qp} \cdot V_{dc1} - S_{qn} \cdot V_{dc2} \end{cases} \quad (8)$$

If equation (8) is replaced in equation (7), then the current equations in the d-q frame will be as in equation (9).

$$L_s \cdot \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -R_s & \omega L_s \\ -\omega L_s & -R_s \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} e_d \\ e_q \end{bmatrix} - \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad (9)$$

It is seen from equation (9) that the instantaneous current components of the d and q axis (i_d and i_q) are coupling. $\omega L i_d$ and $\omega L i_q$ in system are disturbance. It is difficult to design the current controller for the coupling. The decoupled current controller and the voltage feed-forward controller to solve the problem achieving the good control performance is designed in VOC strategy. The VOC block diagram of the three-level rectifier controlled by the space vector PWM based on d-q synchronous rotating axis is shown in the Figure 2 [15].

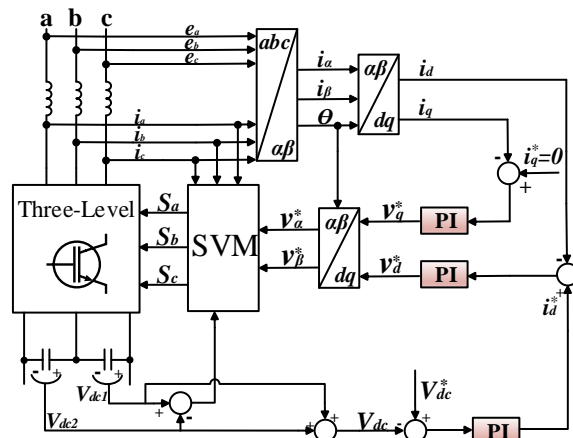


Figure 2. VOC block diagram of three-level rectifier

3. ANALYZING VOLTAGE ORIENTED CONTROL STRATEGY

As the VOC strategy provides decoupled control of active and reactive power with a fast dynamic response, it enables the realization of control in cascade system using PI control blocks both outer voltage and inner current control loops. The inner current control loop is based on the compare the AC current with the AC current reference obtained from the outer voltage control loop. The outer voltage controller is based on the compare the DC voltage reference with the DC voltage and is required to achieve the active power balance [16].

3.1. Inner Current Controller

AC signal are transformed into the DC signal using d-q transformations because it is difficult to control. The general block diagram of inner current control loop given in Figure 3 consist of PI controllers, decoupling factors and feed-forward terms [17].

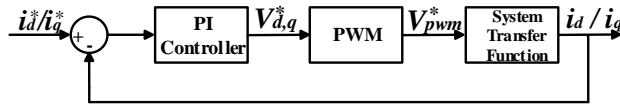


Figure 3. General block diagram of inner current control loop

It is no difference between to design the current controller between d axis with q axis, so the d axis only will be used to design in the paper.

3.1.1. PI Controller

The PI controller minimizes the error to convert from the difference value between the reference (i_d^*) and the measured (i_d) current in steady state, as a result the PI controller increases the stability of the closed loop system [18]. The PI controller converts current error at input to voltage at output. The PI controller is given in equation (10)-(11).

$$PI(s) = K_{ip} + \frac{K_{il}}{s} = K_{ip} \cdot \left(\frac{1 + T_{il} \cdot s}{T_{il} \cdot s} \right) \quad (10)$$

$$(i_d^*(s) - i_d(s)) \cdot \left(K_{ip} + \frac{K_{il}}{s} \right) = V_d(s) \quad (11)$$

The proportional gain K_{ip} and integral time constant $T_{il} = K_{ip} / K_{il}$ are the design parameters to be specified in equation (10)-(11).

3.1.2. PWM

The output voltage of the rectifier, which is considered to be an ideal power converter, is assumed to follow the reference voltage with a time delay T_a . T_a is a half of an average switching cycle T_s . The time delay is expressed in the equation (12).

$$R(s) = \frac{1}{1 + T_a \cdot s} \quad ; \quad T_a = T_s / 2 \quad (12)$$

$$V_d(s) \cdot \frac{1}{(1 + T_a \cdot s)} = V_d^*(s) \quad (13)$$

3.1.3. System Transfer Function

Referring to equation 9, the system model with multi-input and multi-output is nonlinear. The output of the current controllers designed for i_d and i_q are obtained the voltage references which are V_d^* and V_q^* . Using the equations (11) and (13), these reference voltages are obtained as in equation (14).

$$V_d^* = (i_d^* - i_d) \cdot \left(K_{ip} + \frac{K_{il}}{s} \right) \cdot \frac{1}{(1 + T_a \cdot s)} \quad (14)$$

In the d-q frame, the reference voltages of the current controller of the three-phase VSR are given in equation (15).

$$V_d^* = -\left(K_{ip} + \frac{K_{it}}{s}\right)(i_d^* - i_d) + \omega L_s i_q + e_d \tag{15}$$

When the equation (15) is replaced with the equation (13) and the equation obtained is equal to equation (9), the equation (16) is obtained.

$$L_s \cdot \frac{di_d}{dt} + R_s i_d = V_d \tag{16}$$

As seen from equation (16), the coupling is eliminated, i.e. independent control can be made on the d and q axis. If laplace transform is applied to equation (16), the transfer function of the system is obtained as given in the equation (17).

$$\frac{i_d(s)}{V_d(s)} = G(s) = \frac{1}{R_s} \cdot \frac{1}{1 + s\tau} \quad ; \quad \tau = L_s / R_s \tag{17}$$

In the equation (17), τ is time constant of line. The detailed block diagram of the inner current control loops for the d axis and the q axis is given in Figure 4.

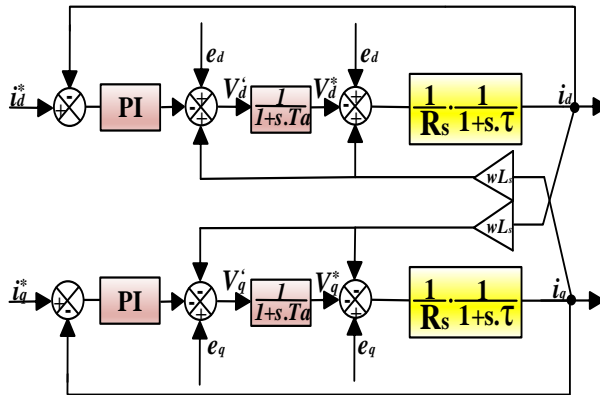


Figure 4. Detail block diagram of the inner current loops for d and q axis

The feed-forward technique is used to eliminate the slow dynamic response in cascade control [19]. The decoupled inner current control loops in per-unit system in Figure 5 can be obtained the reference [18].

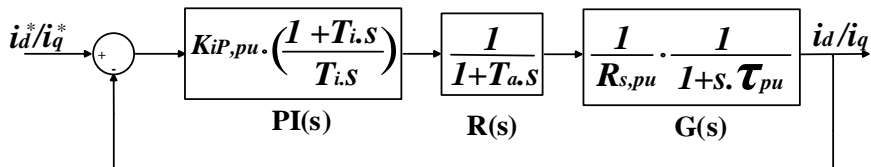


Figure 5. Block diagram of the inner current control loop in per-unit

3.1.4. Tuning of PI Inner Current Controller

The cascade control requires a fast response, so the inner controller must be designed accordingly. As the system contains low order (<3) transfer function the "Modulus Optimum" is used to design the PI parameters in the inner control loop. This method provides fast response and simplicity, as well as relatively low oscillation in the closed loop [18]. The aim of the modulus optimum method is to make the cut-off frequency as high as possible. Hence the internal time constant of the PI controller is designed to cancel out the dominant pole in the system [20]. Referring to Figure 5, the open loop transfer function of per-unit system can be written as the equation (18).

$$G_{C,OL}(s) = K_{iP,pu} \cdot \left(\frac{1+T_{il} \cdot s}{T_{il} \cdot s} \right) \cdot \frac{1}{(1+T_a \cdot s)} \cdot \frac{1}{R_{s,pu}} \cdot \frac{1}{1+\tau_{pu} \cdot s} \quad (18)$$

According to modulus optimum objective, the zero of the open loop transfer function is eliminated by taking $T_{il} = \tau_{pu}$. When the equation (18) is rewritten, the following equation will be obtained;

$$G_{C,OL}(s) = \frac{K_{iP,pu}}{R_{s,pu} \cdot \tau_{pu}} \cdot \frac{1}{s \cdot (1+T_a \cdot s)} \quad (19)$$

The second order closed loop transfer function can be written using the $G_{C,OL}(s)$ given in equation (19). The controller gain is calculated according to the closed-loop transfer function. If the necessary simplifications are made in the last equation, the simplified closed-loop transfer function is obtained in the equation (20).

$$G_{C,CL}(s) = \frac{1}{2T_a^2 s^2 + 2T_a s + 1} \quad (20)$$

The system has damping factor $\xi = \frac{1}{\sqrt{2}}$ and undamped natural frequency $\omega_n = \frac{1}{T_a \sqrt{2}}$.

The PI controller parameter set according to the modulus optimum method can be given as in equation (21).

$$K_{iP,pu} = \frac{R_{s,pu} \cdot \tau_{pu}}{2 \cdot T_a} \quad ; \quad T_{il} = \tau_{pu} \quad (21)$$

After the necessary calculations for the PI parameters, $K_{iP} = 7,8$ and $K_{iI} = 50$ are found.

3.2. Outer Voltage Controller

The overall block diagram of outer voltage controller is shown Figure 6.

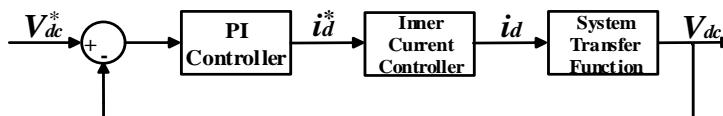


Figure 6. General block diagram of outer voltage control loop

When designing the outer voltage control loop, the closed loop inner current transfer function is assumed to be ideal. Instead of the ideal assumption, the second order current control transfer function given in equation (20) can be simplified as the first order transfer function given in the equation (22) [16].

$$\frac{1}{2T_a^2 \cdot s^2 + 2T_a \cdot s + 1} \cong \frac{1}{T_{ro} \cdot s + 1} \tag{22}$$

where T_{ro} is time integral of difference between the reference and the output of the system and can give as $T_{ro} = 2T_a$.

The PI controller can be designed similar to one in the current control. The power balance between the AC input and the DC output can be given as in the equation (23). Using power balance, the value of the current gain can be found as in the equation (24).

$$P = \frac{3}{2}(V_d \cdot i_d + V_q \cdot i_q) = V_{dc} \cdot I_{dc} \quad ; \quad V_q = 0 \tag{23}$$

$$C_{dc} \cdot \frac{dV_{dc}}{dt} = \frac{3}{2} \cdot \frac{V_d}{V_{dc}} \cdot i_d - I_L \tag{24}$$

The equation (24) is nonlinear. For nonlinear system, linearization should be performed according to Taylor series at working point V_{dc}^* which is specified as the reference input. The disturbing input I_L is omitted from the linearized system and the entrance sign is considered only i_d in the system. The linear expression is written in Laplace form as in the equation (25).

$$\frac{\Delta V_{dc}(s)}{\Delta i_d(s)} = \frac{3}{2} \cdot \frac{V_{d,0}}{V_{dc}^*} \cdot \frac{1}{s \cdot C_{dc}} \tag{25}$$

As the variables in the whole system are processed by simultaneously, the slow dynamic response must be eliminated. Therefore, the feed-forward is used in this study.

The outer voltage controller is used to control the capacitor current so as to maintain the power balance. Thus, the reference value of i_d should be as given in the equation (26) [16].

$$i_d = \frac{2}{3} \cdot \frac{V_{dc}}{V_d} \cdot I_L \tag{26}$$

The detailed block diagram of the outer voltage controller is shown in Figure 7. The terms that form the Figure 7 are written in per-unit values.

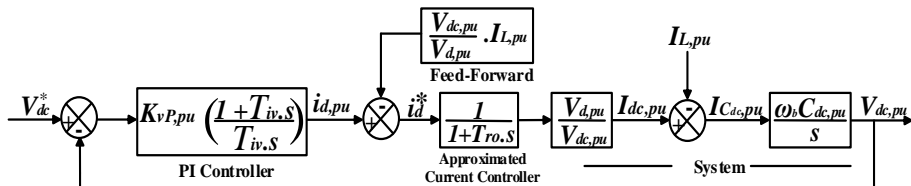


Figure 7. The block diagram of the outer voltage control loop as per-unit

3.2.1. Tuning of PI Outer Voltage Controller

The design objective of the outer voltage controller loop is system stability and optimal regulation. The open loop transfer function of the system given in Figure 7 is derived as the equation (27) by ignoring the disturbance input ($I_{L,pu}$) and feed-forward.

$$G_{V,OL}(s) = K_{vp,pu} \cdot \left(\frac{1 + T_{iv} \cdot s}{T_{iv} \cdot s} \right) \cdot \frac{1}{(1 + T_{ro} \cdot s)} \cdot \left(\frac{V_{d,pu}}{V_{dc,pu}} \cdot \frac{\omega_b \cdot C_{dc,pu}}{s} \right) \quad (27)$$

If the poles of a system are close to origin or at the origin, the modulus optimum method used in the current control loop can not be applied to this system. Therefore, the ‘‘Symmetrical Optimum’’ method mentioned in the literature [16] will be used to design PI parameters of the outer control loop. As this method maximizes the phase margin, it can tolerate more time delays and also optimize disturbance of input. Using the equations $W = V_d/V_{dc}$ and $T_p = 1/\omega_b C_{dc,pu}$ in the equation (27), the equation (28) is obtained.

$$G_{V,OL}(s) = K_{vp,pu} \cdot \left(\frac{1 + T_{iv} \cdot s}{T_{iv} \cdot s} \right) \cdot \frac{W}{1 + T_{ro} \cdot s} \cdot \left(\frac{1}{T_p \cdot s} \right) \quad (28)$$

where $K_{vp,pu} = \frac{T_p}{W \cdot \sqrt{T_{iv} \cdot T_{ro}}}$. After finishing the simplification, the tuning criteria is determined by the symmetrical optimum method as given [18]. The open loop transfer function and the closed loop one is shown in equation (29) and (30), respectively.

$$G_{V,OL}(s) = \frac{1}{a^3 \cdot T_{ro}^2 \cdot s^2} \cdot \left(\frac{1 + a^2 \cdot T_{ro} \cdot s}{1 + T_{ro} \cdot s} \right) \quad (29)$$

$$G_{V,CL}(s) = \frac{1 + a^2 \cdot T_{ro} \cdot s}{a^3 \cdot T_{ro}^3 \cdot s^3 + a^3 \cdot T_{ro}^2 \cdot s^2 + a^2 \cdot T_{ro} \cdot s + 1} \quad (30)$$

where $a = \sqrt{\frac{T_{iv}}{T_{ro}}}$ and $K_{vp,pu}$ can be simplified as $K_{vp,pu} = \frac{T_p}{a \cdot W \cdot T_{ro}}$.

For different values of the pole coefficient a which is seen in equation (30), the different conditions occur in the locus of roots. If the value of a decreases, a small phase margin is obtained which causes high oscillation, or if the value of a increases, better damping but a slower response occur. The recommended value for a is between 2 and 4 in literature [21]. Therefore the PI controller parameter set according to the symmetrical optimum method can be given as $K_{vp} = 0,82$ and $K_{vI} = 50,5$.

4. SPACE VECTOR PULSE WIDTH MODULATION

For the switching status, the equivalent of the three-level PWM rectifier circuit in Figure 1 converts to Figure 8. This circuit structure is called as 'single pole triple throw (SPTT)' in the literature [22].

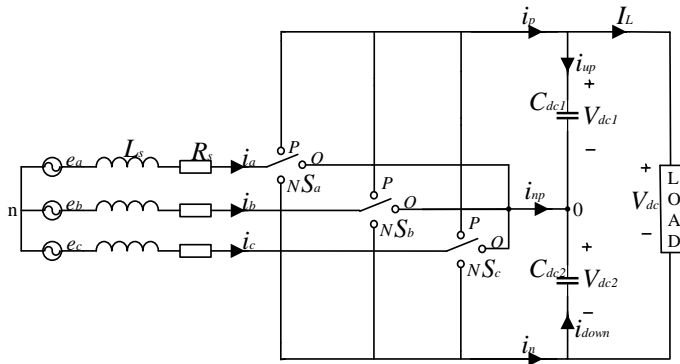


Figure 8. The equivalent circuit of three-level PWM rectifier (SPTT model)

Each phase of three-level rectifier consists of four switches each having three switching status, which can be represented by P, O, N given in Figure 8. As the mathematical operations are made easier, the switching status are given in Table 1.

Table 1. The switching states of three-level NPC rectifier (i=a,b,c)

S_{1i}	S_{2i}	S_{3i}	S_{4i}	Voltage Equivalent
1	1	0	0	$V_{dc}/2$
0	1	1	0	0
0	0	1	1	$-V_{dc}/2$

The three-level rectifier has 27 switching states based on the generalization n^3 . n is the number of levels in the rectifier. Figure 9 shows the voltage vectors corresponding to the 27 switching states of the three-level rectifier.

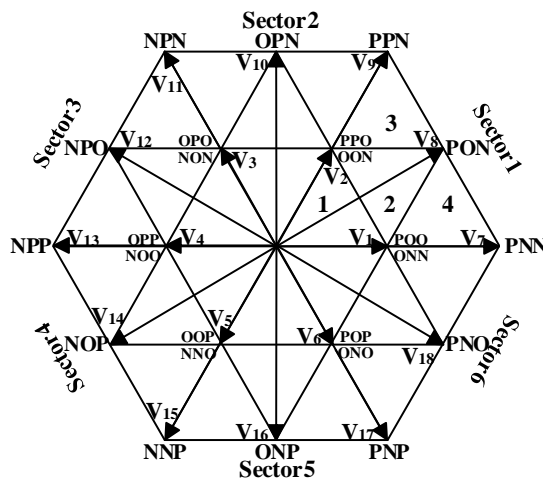


Figure 9. Vector diagram of three-level rectifier

The entire vector space in Figure 9 is divided into 24 triangles. The reference voltage vector V_{ref} , which falls into any region within any sector is created by the closest three vectors surrounding the region where it falls.

The symmetrical structure of the three-level system allows the reduction to the general state of the sector 1 (sector $\pi/3$). For a sufficiently high switching frequency f_s , if the reference voltage vector V_{ref} is assumed to fall to region 2 within sector 1 as shown in Figure 10, the nearest vectors V_1, V_2 and V_8 boarding to this region create the reference voltage vector [23].

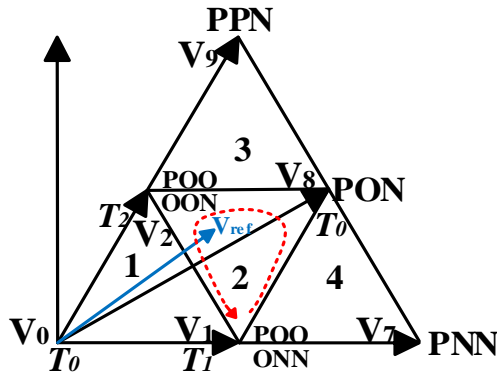


Figure 10. The reference voltage vector falling into region 2 in sector 1

The calculation of switching times is given in the equation (31)-(32) [24].

$$T_1V_1 + T_2V_2 + T_0V_8 = T_sV_{ref} \quad (31)$$

$$T_0 + T_1 + T_2 = T_s \quad (32)$$

T_0, T_1 and T_2 given in equation (31) are respectively switching times of vectors V_1, V_2 and V_8 for given a period. The values of the switching times given in equation (32) are shown in the equation (33)-(35).

$$T_0 = 2k \sin\left(\frac{\pi}{3} + \theta\right) - T_s \quad (33)$$

$$T_1 = T_s - 2k \sin \theta \quad (34)$$

$$T_2 = T_s - 2k \sin\left(\frac{\pi}{3} - \theta\right) \quad (35)$$

where, k is given in equation (36).

$$k = \frac{2m_n}{\sqrt{3}} T_s \quad (36)$$

where m_n is modulation index:

$$m_n = \frac{|V_{ref}|}{\frac{2}{3}V_{dc}} \tag{37}$$

The procedure for calculating switching times in region 2 of sector 1 can be applied in the same way to other regions. The switching times for all regions of sector 1 are given in Table 2.

Table 2. The switching times in sector 1

Region Time	1	2	3	4
T_0	$T_s - 2k \sin\left(\frac{\pi}{3} + \theta\right)$	$2k \sin\left(\frac{\pi}{3} + \theta\right) - T_s$	$2k \sin\left(\frac{\pi}{3} - \theta\right)$	$2k \sin \theta$
T_1	$2k \sin\left(\frac{\pi}{3} - \theta\right)$	$T_s - 2k \sin \theta$	$2k \sin \theta - T_s$	$2T_s - 2k \sin\left(\frac{\pi}{3} + \theta\right)$
T_2	$2k \sin \theta$	$T_s - 2k \sin\left(\frac{\pi}{3} - \theta\right)$	$2T_s - 2k \sin\left(\frac{\pi}{3} + \theta\right)$	$2k \sin\left(\frac{\pi}{3} - \theta\right) - T_s$

After the switching times are calculated, the switching cycle must also be determined. The switching cycle is important for SVPWM because it directly affects THD and switching losses. To optimize the switching cycle, it is more convenient method to make the switching cycle symmetrical and to use the same switching state at both the beginning and end of the cycle. The rectifier still has undesirable switching states. In order to minimize the harmonic distortion, it is necessary to eliminate unnecessary switching states. Therefore, all switching times are arranged to generate the optimal switching cycle. The switching is done by changing the status of a single switch at given a time [23, 24]. For an example, the most appropriate switching cycle for the region 2 of sector 1 is given in Figure 11.

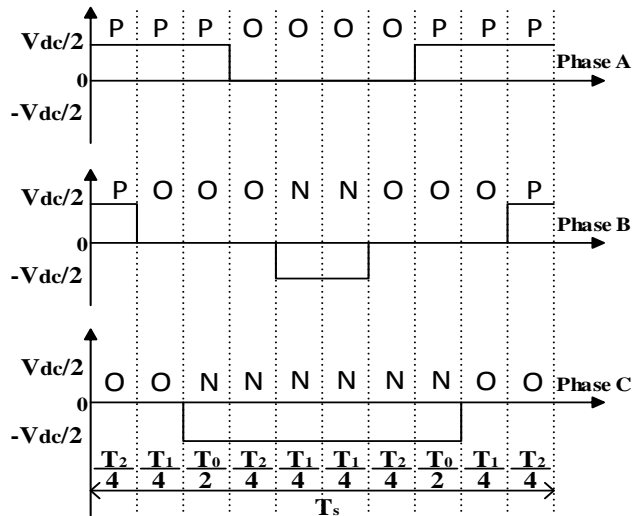


Figure 11. The switching cycle for region 2 of sector 1

The PWM signals driving the switches are generated by SVPWM control algorithm that included dq frame. For this aim, symmetrical PWM generating will be designed.

4.1. Symmetrical PWM Generating

Each phase of the three-level rectifier has three voltage levels (P, 0, N). According to the symmetrical PWM generating, two PWM generators are required to generate the driving signal for the four switches in each phase. Taking phase A in Figure 11 as an example, the waveform can be thought of in two ways. The former includes switching times in which only P exists. The latter includes switching times in which only N disappear. This is shown in Figure 12. According to the symmetrical pattern, the PWM driving times of each switch in all region of sector 1 can be achieved as given in Table 3 [25].

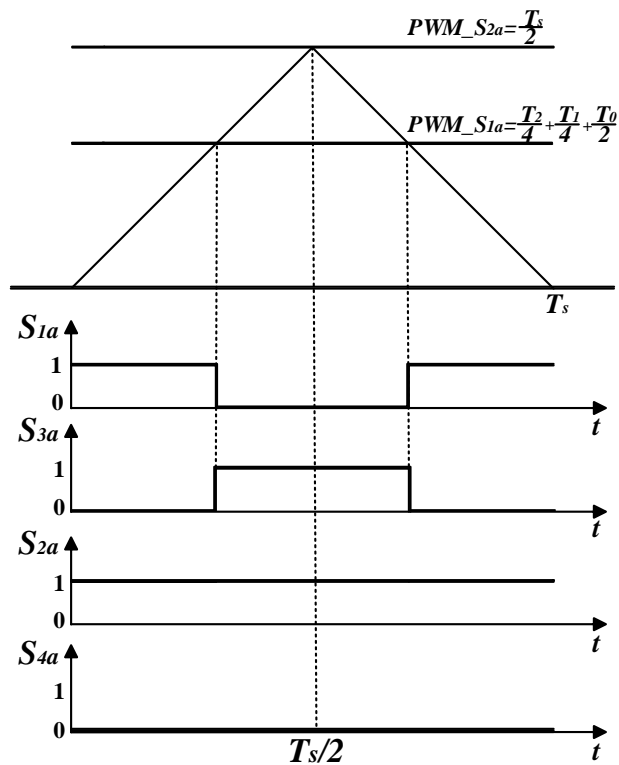


Figure 12. The driving time setting for four switching using two PWM generators in phase A

Table 3. The PWM driving setting for each switch of upper arms in sector 1

Region Time	1	2	3	4
PWM_{S1a}	$\frac{T_2 + T_1}{4}$	$\frac{T_2 + T_1 + T_0}{4 + \frac{1}{2}}$	$\frac{T_s - T_2}{2 - 4}$	$\frac{T_s - T_1}{2 - 4}$
PWM_{S2a}	$\frac{T_s}{2}$	$\frac{T_s}{2}$	$\frac{T_s}{2}$	$\frac{T_s}{2}$
PWM_{S1b}	$\frac{T_2}{4}$	$\frac{T_2}{4}$	$\frac{T_2 + T_1}{4 + \frac{1}{2}}$	0
PWM_{S2b}	$\frac{T_s - T_1}{2 - 4}$	$\frac{T_s - T_1}{2 - 4}$	$\frac{T_s}{2}$	$\frac{T_1 + T_0}{4 + \frac{1}{2}}$
PWM_{S1c}	0	0	0	0
PWM_{S2c}	$\frac{T_s - T_1 - T_2}{2 - 4 - \frac{1}{4}}$	$\frac{T_2 + T_1}{4 + \frac{1}{4}}$	$\frac{T_2}{4}$	$\frac{T_1}{4}$

The symmetrical PWM generation applied above for sector 1 is likewise applicable to other sectors. However, the voltage vector and switching times are totally different for the 24 regions that make up the space vector. Therefore, it becomes difficult to calculate switching times and sequences. Since there is a close relationship between sectors, a simplified algorithm can make the calculation easier. That is, it is enough to use only two PWM signals to calculate the driving time of the four switches in each phase.

There is 60° among each sector. Sector 1 is used as a reference for switching time calculating in other regions of any other sector. The equation (31) has been gave switching time for region 2 of sector 1. As in the equation (31), the switching time calculation can be generated for any region of any sector. When the relationship of 60° is considered, sector N is equal to sector 1 when multiplied by $e^{-j(N\pi/3)}$ (N=1,2,3,4,5).

The reference voltage vector for sector 1 is expressed in the equation (38).

$$V_{ref}^1 = \frac{2}{3}(e_a + e_b \cdot e^{\frac{2}{3}j\pi} + e_c \cdot e^{-\frac{2}{3}j\pi}) \tag{38}$$

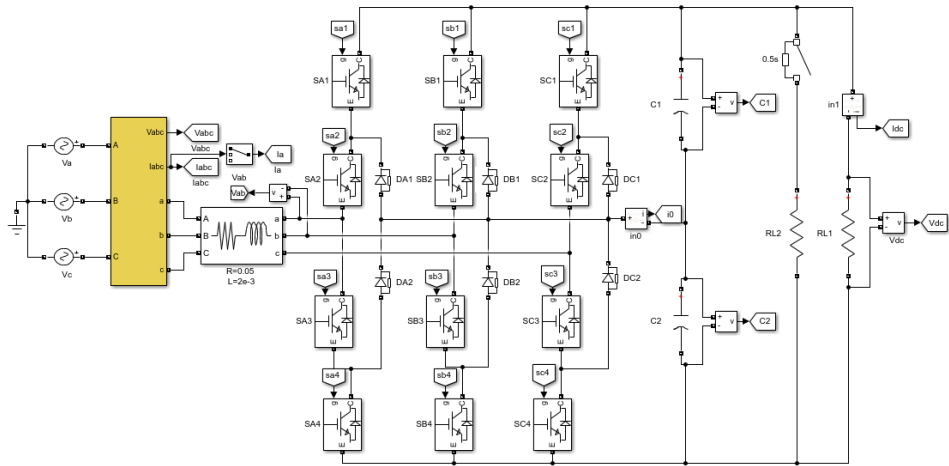
Referring to equation (38) and simplification algorithm, the reference voltage vector for sector 2 can be written as equation (39).

$$V_{ref}^2 = V_{ref}^1 \cdot xe^{\frac{\pi}{3}j} = \frac{2}{3}(-e_b - e_c \cdot e^{\frac{2}{3}j\pi} - e_a \cdot e^{-\frac{2}{3}j\pi}) \tag{39}$$

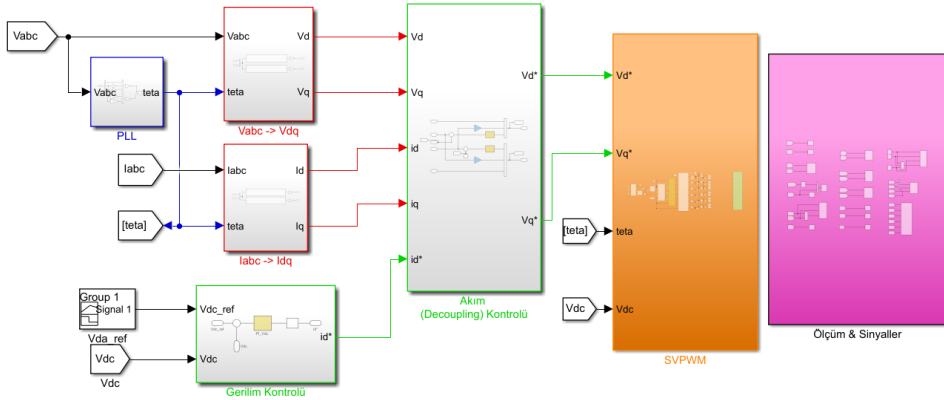
5. SIMULATION RESULTS

The simulation model generated in the Matlab / Simulink program of the three-level rectifier controlled by the space vector PWM is shown in Figure 13.

Control structures consisting of outer voltage and inner current loop using the simulink model are shown in Figure 14. As the effects of the coupled components have been eliminated in the current control loop, the currents can be independently controlled.



(a)



(b)

Figure 13. Matlab/Simulink simulation of three-level space vector PWM rectifier

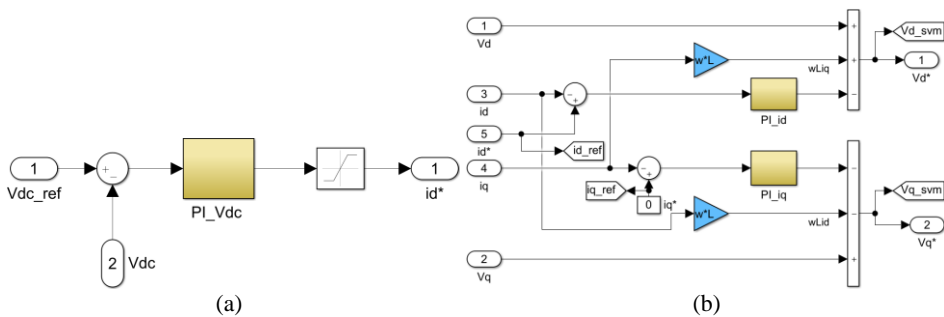


Figure 14. (a) The outer voltage loop (b) The inner current loop

The d-q synchronous rotating axis voltages V_d^* and V_q^* are both the control output vectors and also will form the reference voltage vector in the space vector. In Figure 15, the internal structure of the space vector PWM block is shown.

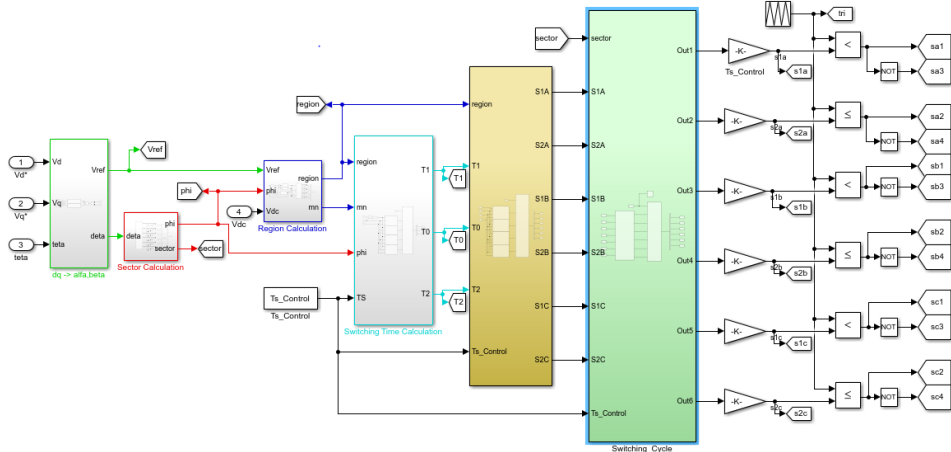


Figure 15. PWM block diagram of space vector

Table 5 shows the parameter values of the three-level rectifier circuit simulated.

Table 5. Circuit parameter values of three-level rectifier

Grid phase-neutral voltage; V_{a_rms}	220 V	Line inductance; L	2 mH
Grid frequency	50 Hz	DC capacitance; C_1, C_2	750 μ F
Line resistance; R	0.05 Ω	Load resistance; R_L	50 Ω
Reference voltage; V_{dc_ref}	600 V	Switching frequency; fs	5 kHz

5.1. Normal Operating Status

In Figure (16)-(20), the space vector PWM is applied to the three-level rectifier in normal operation. The accuracy and efficiency of both the outer voltage closed loop controllers and the inner current ones have been tested.

As shown in Figure 16, it is seen that the output voltage V_{dc} has a reference voltage value of 600 V in a short time of 0.05s and the output voltage V_{dc} has a small ripple, such as ± 0.2 V in steady state.

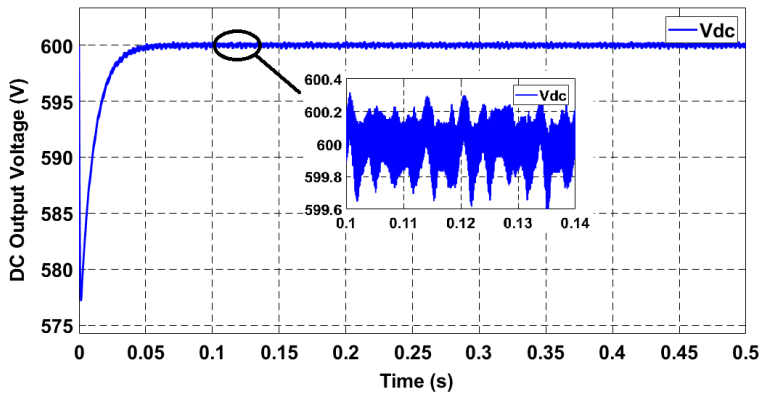


Figure 16. The DC output voltage (V_{dc})

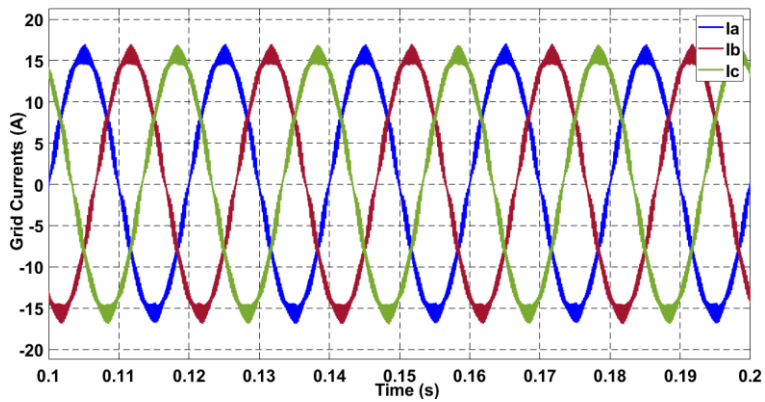


Figure 17. Three-phase grid currents

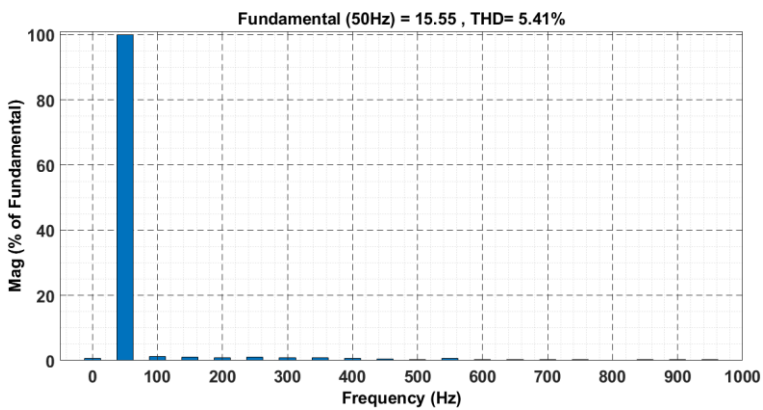


Figure 18. THD analysis graph of phase A

The three-phase grid currents are close to the sinusoidal form in Figure 17, therefore the power factor is close to maximum. As shown in Figure 18, THD value of the phase current A is 5.41%. In this case, the maximum active power is consumed by the load.

It is not preferred to design a separate filter to the input to understand what the actual performance of the circuit is. In addition, passive elements are used in the active filter to reduce the cost. Therefore, the THD value was slightly higher than the 5% standard. THD value can be reduced by designing a low cost circuit.

As shown in Figure 19, two DC output capacities, C_1 and C_2 , share the 600V output voltage equally. This sharing will reduce the voltage stress (dV/dt) on the switches in each phase.

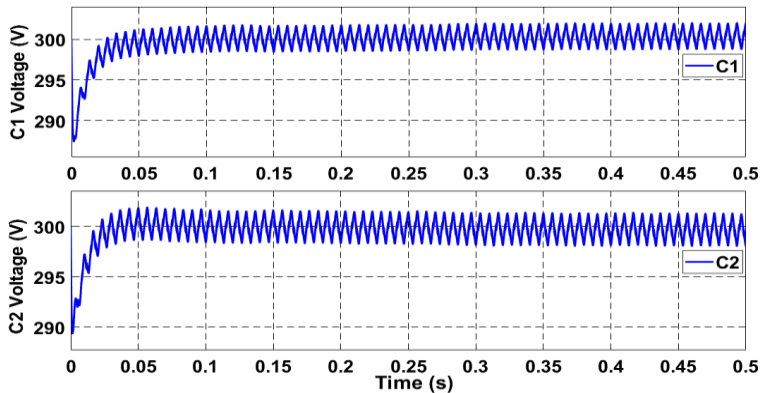


Figure 19. Capacitor voltages C_1 and C_2

Figure 20 shows the phase-to-phase voltage V_{ab} on the input side of the rectifier. While the phase-to-phase voltage waveform is 3 level in a two-level rectifier, three-level rectifier's is 5 level. Therefore, the harmonic performance of the three-level rectifier is better than the two-level rectifier [2].

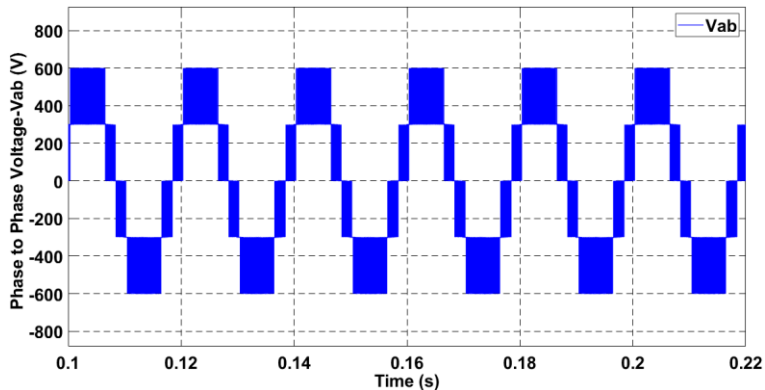


Figure 20. The voltage V_{ab} between phases a and b

5.2. Load Change Status

In order to analyze the performance of the space vector PWM control under transient conditions, the load is suddenly changed from 50 ohms to 25 ohms ($t=0.2s$). As the load value is changed, the output voltage also varies. The grid phase currents, the capacities voltages on the DC side and phase-to-phase voltage in this case are shown in Figure 21-24.

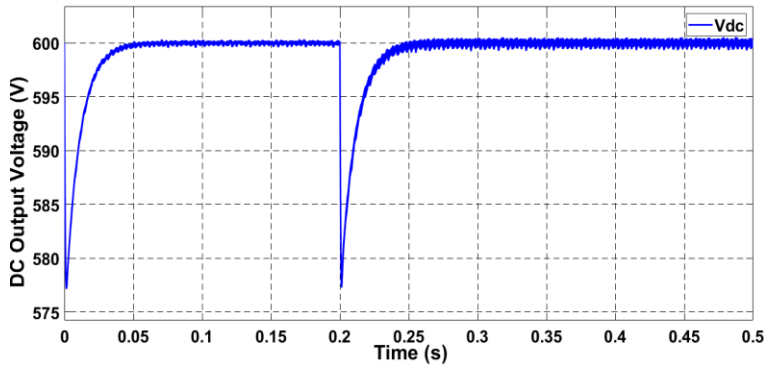


Figure 21. The output voltage V_{dc} in case of the load changing suddenly

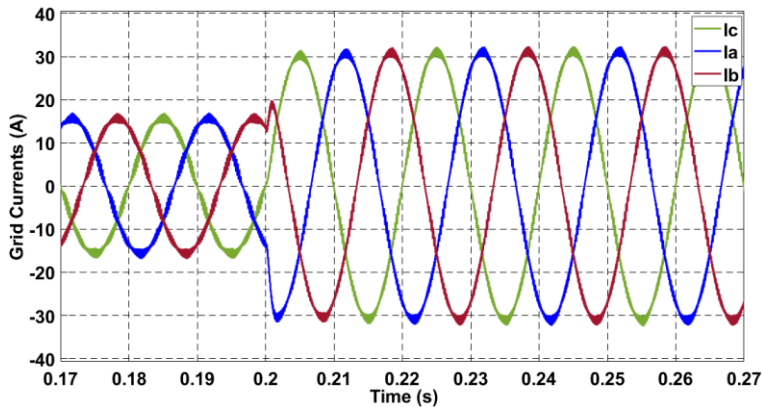


Figure 22. Three-phase grid currents in case of the load changing suddenly

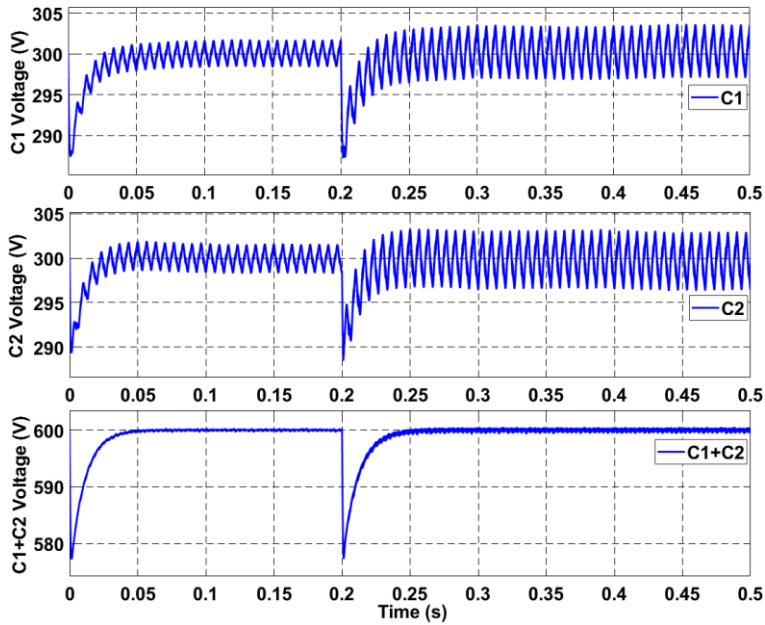


Figure 23. The capacitor voltages C_1 , C_2 and $C_1 + C_2$ in case of the load changing suddenly

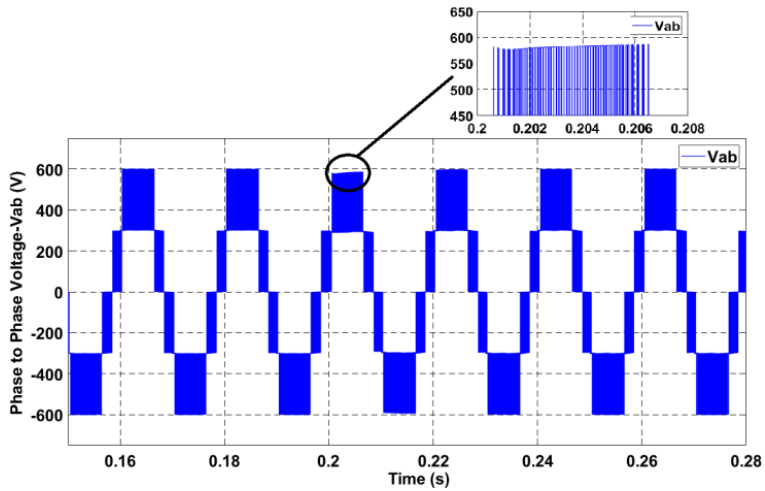


Figure 24. The phase-to-phase voltage V_{ab} in the case of the load changing suddenly

When load changes ($t = 0.2s$), it is clearly seen that the space vector PWM control responds rapidly and keeps the system stable. Furthermore, it is seen that the designed system reduces the THD value of the grid current and the desired reference voltage value is maintained at the output.

5.3. Reference Voltage Change Status

In order to analyze the performance of the space vector PWM control under transient conditions, it is investigated that the desired reference voltage at the DC output is reduced to 550 V at $t = 0.2$ s and increased to 700 V at $t = 0.4$ s. The changes in the output voltage, the grid phase currents, the capacity voltages on the DC side and the phase-to-phase voltage in this case are shown in Figure 25-28.

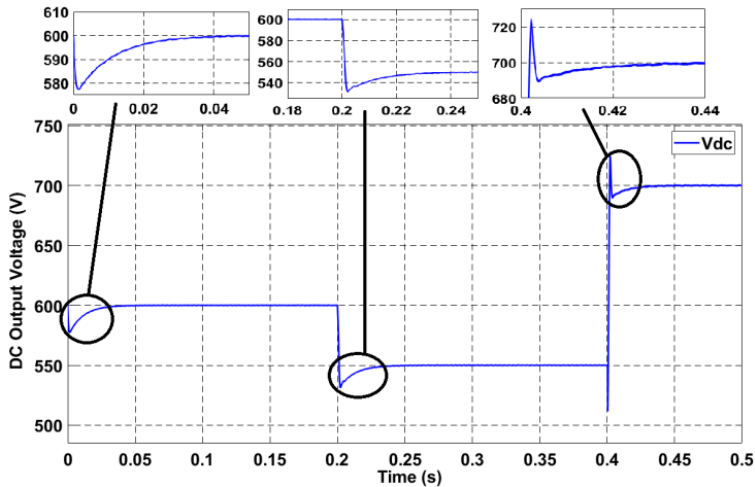


Figure 25. The output voltage V_{dc} in case of the changing of the reference voltage value

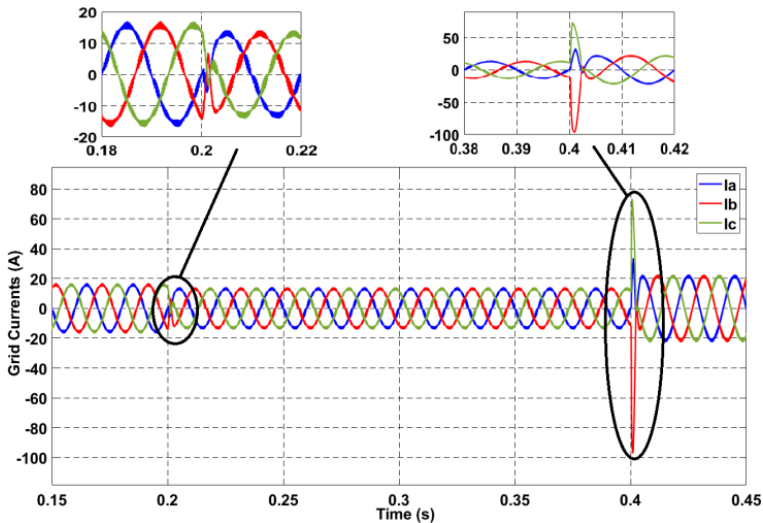


Figure 26. Three-phase grid currents in case of the changing of the reference voltage value

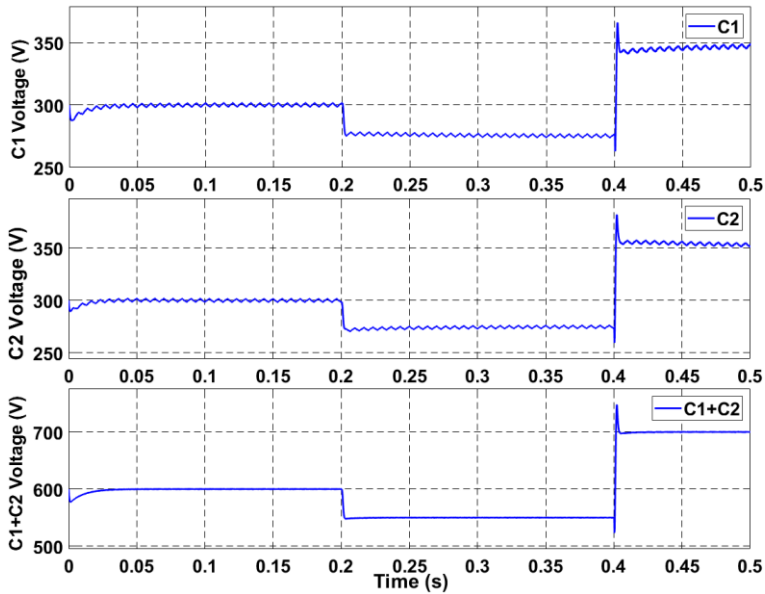


Figure 27. The capacitor voltages C_1 , C_2 and $C_1 + C_2$ in case of the changing of the reference voltage value

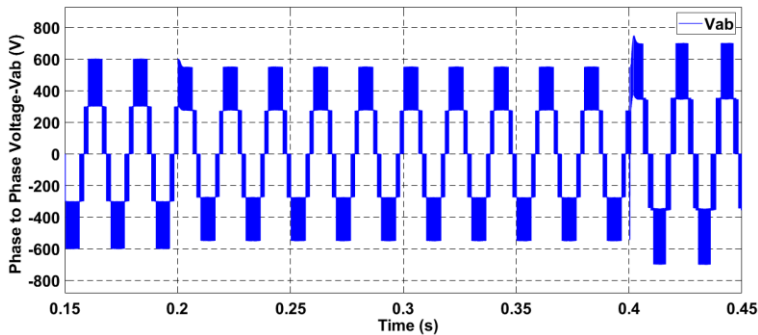


Figure 28. The phase-to-phase voltage V_{ab} in the case of the changing of the reference voltage value

6. CONCLUSION

In this study, an SVPWM control algorithm based on the d-q synchronous rotating axis set of the three-level rectifier is proposed. It is shown that the SVPWM reduces the harmonics in the sinusoidal input current of the three-level rectifier, increases the power factor and keeps the DC output voltage constant at the desired value. It is achieved that the simplified SVPWM algorithm used to calculate switching times and sequences has a significant advantage according to conventional SVPWM. It is checked whether the three-level NPC rectifier performs voltage and current control correctly and it is seen that PI controller responds to abnormal operating conditions fast, stable and dynamic. It is found that symmetric optimum and modulus optimum methods facilitate the design of outer voltage and inner current controllers, respectively. In the

literature, it is seen that this rectifier, which has a bi-directional power flow characteristic, works stable as an inverter [26]. The simulation results showed that the three-level rectifier controlled by the space vector PWM technique discussed in this study provides the desired performance.

REFERENCES

- [1] Arifoğlu, U. (2002). Güç sistemlerinin bilgisayar destekli analizi (problem çözümlü). Alfa.
- [2] Song, W. X., Cao, D. P., Qiu, J. Y., Chen, C., & Chen, G. C. (2009, May). Study on the control strategy of three-level PWM rectifier based on SVPWM. In 2009 IEEE 6th International Power Electronics and Motion Control Conference (pp. 1622-1625). IEEE.
- [3] Wu, H., Liu, T., Yang, T., Wang, J., Ding, S., & Xing, Y. (2017, October). A modified SVPWM strategy applied to a three-phase three-port bidirectional AC-DC rectifier for efficiency enhancement. In 2017 IEEE Energy Conversion Congress and Exposition (ECCE) (pp. 3420-3426). IEEE.
- [4] He, X., Han, P., Lin, X., Wang, Y., & Peng, X. (2018, May). SVPWM strategy based on multilevel 3LNPC-CR. In 2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia) (pp. 1027-1031). IEEE.
- [5] Cichowlas, M. (2004). PWM rectifier with active filtering. Warsaw University of Technology, Warsaw.
- [6] Mukherjee, D., & Kastha, D. (2018). A reduced switch hybrid multilevel unidirectional rectifier. *IEEE Transactions on Power Electronics*, 34(3), 2070-2081.
- [7] Lu, T., Zhao, Z., Zhang, Y., Zhang, Y., & Yuan, L. (2008, October). A novel direct power control strategy for three-level PWM rectifier based on fixed synthesizing vectors. In 2008 International Conference on Electrical Machines and Systems (pp. 1143-1147). IEEE.
- [8] Jayaram, N., Agarwal, P., & Das, S. (2012, December). A Three Phase five level cascaded H-Bridge rectifier with zero current injection scheme. In 2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)(pp. 1-7). IEEE.
- [9] Watson, A. J., Wheeler, P. W., & Clare, J. C. (2007, September). A selective harmonic elimination system for restoring and equalising DC link voltages in a multilevel active rectifier. In 2007 European Conference on Power Electronics and Applications(pp. 1-7). IEEE.
- [10] Sharma, A. K., Mishra, V., Kaushik, N., Singhal, M., & Sharma, A. (2013). Advanced Techniques for Controlling Output Voltage of Inverter. *International Journal of Electronics and Communication Engineering*, 3(2).
- [11] Rashid, M. H. (Ed.). (2017). *Power electronics handbook*. Butterworth-Heinemann.
- [12] Nabae, A., Takahashi, I., & Akagi, H. (1981). A new neutral-point-clamped PWM inverter. *IEEE Transactions on industry applications*, (5), 518-523.
- [13] Lu, T., Zhao, Z., Zhang, Y., & Yuan, L. (2009, May). A novel direct power control strategy with wide input voltage range for three-level PWM rectifier. In 2009 IEEE 6th International Power Electronics and Motion Control Conference (pp. 897-902). IEEE.
- [14] Draou, A. (2013). A Space Vector Modulation Based Three-level PWM Rectifier under Simple Sliding Mode Control Strategy. *Energy and Power Engineering*, 5(03), 28.
- [15] Phankong, N., Yuktanon, N., & Bhummittipich, K. (2014). Design of Power Rectifier Circuit for Three-Level Back-to-Back Converter. *Energy Procedia*, 56, 574-583.
- [16] Bajracharya, C., Molinas, M., Suul, J. A., & Undeland, T. M. (2008). Understanding of tuning techniques of converter controllers for VSC-HVDC. In *Nordic Workshop on Power and Industrial Electronics (NORPIE/2008)*, June 9-11, 2008, Espoo, Finland. Helsinki University of Technology.
- [17] Muriuki, J., Muriithi, C. M., Ngoo, L., & Nyakoe, G. N. (2016). Wider range of tuning the

- proposed VSC-HVDC system for improved controller performance.
- [18] Setiawan, I., Facta, M., Priyadi, A., & Purnomo, M. H. (2017). Investigation of symmetrical optimum PI controller based on plant and feedback linearization in grid tie inverter systems. *International Journal of Renewable Energy Research*, 7(3), 1228-1234.
 - [19] Kalitjuka, T. (2011). Control of voltage source converters for power system applications (Master's thesis, Institutt for elkraftteknikk).
 - [20] Abildgaard, E. N., & Molinas, M. (2012). Modelling and control of the modular multilevel converter (MMC). *Energy Procedia*, 20, 227-236.
 - [21] Machaba, M., & Braae, M. (2003). Explicit damping factor specification in symmetrical optimum tuning of PI controllers. In *Proc. of First African Control Conference* (pp. 3-5).
 - [22] Gao, S. H., & Qian, X. L. (2014, May). Research on modelling and control of three-level PWM rectifier system. In *The 26th Chinese Control and Decision Conference (2014 CCDC)* (pp. 3813-3817). IEEE.
 - [23] Tong, J., Liu, L. J., Qiao, J. W., Zhang, Q., & Lu, Y. (2018, May). Study of three-level SVPWM algorithm for 60° coordinate system. In *2018 13th IEEE Conference on Industrial Electronics and Applications (ICIEA)* (pp. 2445-2449). IEEE.
 - [24] Deng, Q., & Ge, X. (2019, May). Unified SVPWM Strategy for Post-fault Three-level NPC Voltage Source Inverters. In *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019-ECCE Asia)* (pp. 3090-3095). IEEE.
 - [25] Hu, H., Yao, W., & Lu, Z. (2007). Design and implementation of three-level space vector PWM IP core for FPGAs. *IEEE Transactions on power electronics*, 22(6), 2234-2244.
 - [26] Zhang, Z., Xie, Y. X., Le, J. Y., & Chen, L. (2009, November). Lyapunov-based control for single-phase three-level NPC AC/DC voltage-source converters. In *2009 International Conference on Electrical Machines and Systems* (pp. 1-4). IEEE.

Copyright of Sigma: Journal of Engineering & Natural Sciences / Mühendislik ve Fen Bilimleri Dergisi is the property of Sigma: Journal of Engineering & Natural Sciences / Mühendislik ve Fen Bilimleri Dergisi and its content may not be copied or emailed to multiple sites or posted to a listserv without the copyright holder's express written permission. However, users may print, download, or email articles for individual use.