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Novel three-level T-type isolated bidirectional DC–DC converter

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Abstract: This study presents a novel three-level T-type isolated bidirectional DC–DC converter (3LTT-IBDC) for bidirectional DC power transfer. Owing to of the T-type structure of the proposed converter it has less number of switches and thus, lower cost and higher efficiency, as well as easy control are the advantages of the proposed converter compared to three-level counterparts. Additionally, 3LTT-IBDC is more reliable than three-level converters since unequal voltage blocking does not occur in T-type structure. Moreover, the symmetrical operation of the isolation transformer due to three-level symmetrical voltage waveform, lower voltage stress of switches and thus, higher efficiency are other advantages of 3LTT-IBDC compared to two-level counterparts. Here, the DC voltage gain and power transfer characteristic of the proposed converter for steady-state operation and the expressions of the leakage inductance are derived. The proposed converter is simulated using PSIM. A 2-kW prototype is built to verify the theoretical analysis of the converter. Theoretical and experimental results show a good agreement and validate the competency of the presented converter design. The efficiency of the proposed converter and switching transitions of the switches are analysed. The full load and maximum efficiency of the converter are measured as 96.27% and 96.81%, respectively.

1 Introduction

Increasing electricity demands, environmental problems and potential energy crisis concerns make hybrid systems based on renewable energy sources attractive due to their availability, abundance and safety. However, all renewable energy sources have random output characteristics and thus need an energy storage system to provide more reliable power. Therefore, bidirectional DC-DC converters are essential for renewable energy sources [1].

Isolated bidirectional DC–DC converters have a number of advantages in comparison to non-isolated converters in terms of reliability, soft switching and buck/boost ratio [2, 3]. Voltage-fed dual active bridge (DAB) is one of the most popular isolated bidirectional DC–DC converter topologies due to the easier implementation of single-phase shift control. However, the disadvantage of this topology is the high circulation loss when the primary and secondary voltages of the transformer are not equal [4, 5].

Three-level topologies have many advantages compared to two-level topologies in terms of efficiency and voltage stress on switches [6, 7]. Three-level topologies are mainly divided into two topologies: T-type and I-type. The conduction losses of T-type are less than I-type since there is an extra switch on the transmission path causing more voltage drop in I-type [8, 9]. On the other hand, two vertical-connected switches are subjected to all bus voltages and horizontal-connected switches are subjected to half of the bus voltages in T-type whereas all switches are subjected to half of the bus voltage in I-type. Although low voltage stress on switches indicates that switching losses will be less, the efficiency survey on inverter and rectifier topologies states that the total efficiency in T-type is higher than I-type [10]. Furthermore, direct switching from positive voltage level to negative voltage level is often neglected, and uneven blocking voltage across the switches can be temporarily seen if series switches are closed at the same time in I-type. However, these undesirable effects do not occur in T-type. Therefore, there is no need to create low-level balanced voltage across serial-connected switches, in order to balance transient voltage fluctuations or compensate this transient fluctuation in T-type, which makes T-type topology more reliable [11]. In addition to its reliability, T-type also provides cost advantage [12, 13]. T-type combines the many advantages of two-level topologies such as low conduction losses and low number of circuit elements, with the advantages of a three-level I-type [14]. Compared with I-type, T-type has also many advantages such as symmetrical loss distribution, low harmonic distortion, less gate drivers etc. [15].

There are several studies in the literature examining different three-level isolated bidirectional DC–DC converters structures. For example, a structure using I-type topology in the primary side of the transformer and two-level full-bridge topology in the secondary side has been studied in [16]. Three-level bidirectional half-bridge DC-DC converter performance has been analysed in [17]. In the study, the performance of the half-bridge converter is found to be like traditional DAB due to its remaining operation under two-level modulation strategy and simultaneous opening or closing of the external and internal switches. Furthermore, three-level modulation to the primary side, and two-level modulation to the secondary side have been applied in order to achieve control flexibility [18]. However, the modulation method must be changed when the power is required to be transferred back. A structure using half- and full-bridge topologies with both I-type primary and I-type secondary side of the transformer has also been studied in [19, 20] that examine the control strategy and zero voltage switching (ZVS) of these topologies. In addition, the other structures have also been studied in the literature which are T-type only in the primary side of the transformer in [21] and T-type only in the secondary side of the transformer in [22–24]. Also, T-type switching combination topologies are stated in [24] as more efficient topology than I-type.

There is no study in the literature about isolated bidirectional DC–DC converter which consists of T-type topology on both sides of the isolation transformer. This paper provides a study of a novel three-level T-type isolated bidirectional DC–DC converter (3LTT-IBDC). Unlike traditional isolated bidirectional DC–DC converter, the proposed design consists of T-type switching combination on both sides of the transformer and thus, provides high efficiency, low cost and high reliability, which also make the proposed design a good alternative to conventional converters. In the paper, steady-state analysis, to understand operating principle of the converter, as well as the voltage gain analysis has been provided. In addition, the power transfer characteristic of the converter in continuous conduction mode (CCM) and the expression of the leakage

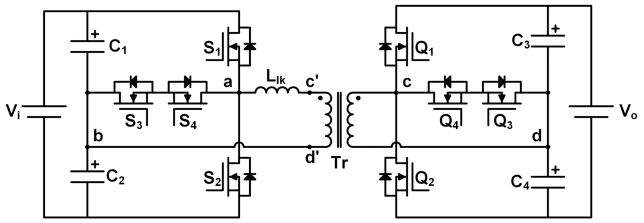


Fig. 1 *Schematic diagram of the proposed converter*

inductance, which is critical for power transfer, are derived in this paper. The proposed converter is also simulated based on theoretical calculations, which is also used to establish the 2-kW laboratory prototype for validation as a final part of the presented study. Voltage gain, power transfer characteristic, voltage stress as well as the switching transition of switches of the proposed converter are then investigated in the experimental study. Finally, the efficiency of the proposed converter is also analysed in the paper for the load conditions between 20 and 100%. The theoretical, measured and experimental results presented in the paper show a good agreement with each other.

The paper is organised as follows: the topology, modulation method and operating principle of the proposed converter are explained in Section 2 in addition to its major operating characteristics such as voltage gain and power transfer. Section 3 describes the operating principle of the proposed converter using PSIM simulation. Section 4 presents experimental results used for validation of the proposed converter design. Lastly, the conclusions of the paper are presented in Section 5.

2 Proposed T-type DC–DC converter

2.1 Topology

The proposed 3LTT-IBDC consists of a high-frequency transformer and three-level T-type switches positioned in the primary and secondary part of the transformer. The circuit diagram of the proposed converter is shown in Fig. 1.

The proposed 3LTT-IBDC has an external inductance (L) connected to the transformer leakage inductance. This external inductance is used for power transfer. The transformer's leakage inductance together with external inductance is illustrated in the circuit diagram in Fig. 1 as leakage inductance L_{lk}. The central point of input capacitors C_1 and C_2, b, is the clamping point of the primary circuit, and voltages across these capacitors are half of the input voltage (V_i). The similar situation is also valid for the secondary side of the circuit. The central point of output capacitors C_3 and C_4, d, is the clamping point of the secondary circuit, and voltages across these capacitors are half of the output voltage (V_o). Therefore, DC input and output voltages applied to the primary and secondary circuits of the DC–DC converter are transformed into three-level, high-frequency AC voltages at $a-b$ and c–d nodes depending on modulation method. Three-level voltage waveforms of nodes $a-b$ and c–d are illustrated in Fig. 2.

2.2 Modulation method

The power transfer in bidirectional converters can be controlled by changing the duty cycle of main switches and/or phase shift ratio between two bridges. For the convenience of this paper, the duty cycle of switches in the bridge is kept constant. Power transfer is provided by changing phase shift ratio between two bridges. For this purpose, the duty cycle (D) of main switches (S_1, S_2, Q_1, Q_2) is fixed to be less than 50%. The duty ratio of auxiliary switches (S_3, S_4, Q_3, Q_4) is 50%. The direction and amplitude of the transferred power in the proposed converter are controlled by the phase shift ratio (δ) in which the phase and amplitude of the voltage $v_{Llk}(t)$ across the equivalent leakage inductance are changed by changing the sign and amplitude of δ. If the phase of the primary voltage $v_{ab}(t)$ is forward according to the phase of the secondary voltage $v_{cd}(t)$, then the net power flow direction is from the primary side to the secondary side. Otherwise, the net power flow is in opposite direction.

In Fig. 2, $V_G S_{(x-y)}$ and $V_G Q_{(x-y)}$, $(x,y = 1,2,3,4)$, are the driving signals of the primary and secondary side switches, $v_{Llk}(t)$ is the multi-level voltage across the leakage inductance, $v_{S1}(t)$, $v_{S3}(t)$, $v_{Q1}(t)$, $v_{Q3}(t)$ are the drain-source voltages, and $i_{S1}(t)$, $i_{S3}(t)$, $i_{Q1}(t)$, $i_{Q3}(t)$ are the drain currents of the corresponding switches and $i_{C3}(t)$ is the current of the C_3 capacitor. The voltage waveforms of the S_1–S_2 and S_3–S_4 are the same but there is π rad phase difference between them. This case is also the same for secondary side switches. Fig. 2 shows that the voltage stress on S_1 and S_2 is equal to V_i while the voltage of S_3 and S_4 is equal to half of V_i. Similarly, the voltage stress of Q_1 and Q_2 is equal to V_o while the voltage stress of Q_3 and Q_4 switches is equal to half of V_o.

2.3 Operating principles in steady-state condition

While explaining the working principle of the proposed 3LTT-IBDC, it is assumed that all circuit elements are ideal, and the circuit works in the steady-state condition. Furthermore, only the power flow from the primary to the secondary side is studied in this paper because of the operating principle of the proposed converter does not change with the direction of the power flow. The difference between these power flows is the sign of δ, which is negative for the power flow from the secondary side to the primary side. Therefore, just a resistance is used to substitute V_o as a consumer when analysing the converter. The 3LTT-IBDC converter has three main operating modes; discontinuous conduction mode, boundary conduction mode (BCM) and CCM. Only CCM will be explained in this paper as the other modes are similar to CCM. Furthermore, CCM operation of the circuit will be given only for the first half period ($T_{sw}/2$), as it is the same as the second half period where T_{sw} is the switching period. CCM operation can be explained in four sub-modes for the first half period that are defined as Mode_0, Mode_1, Mode_2, Mode_3.

Mode_0 ($t_0 - t_1$ time interval): Operating period of Mode_0 is $(D + \delta - 0.5)T_{sw}$; starts with S_1 turning on and ends with Q_2 turning off as illustrated in Fig. 2. The inductance current at t_0 is negative and its value is $i_{Llk}(t_0)$. S_1 turns on at t_0. The new active current path generated with S_1 turning on and its reduced circuit diagram is shown in Figs. 3(a-1) and (a-2), respectively. $v_{ab}(t)$ is equal to $V_i/2$ whereas the primary referred value of $v_{cd}(t)$ is equal to $-nV_o/2$, as seen from the reduced circuit diagram in Fig. 3(a-2), where n is transformer turn ratio. Therefore, as soon as S_1 turns on, the inductance voltage becomes $(V_i + nV_o/2)$. After that time, the inductance current increases by $((V_i + nV_o)/(2L_{lk}))$ inclination and reaches to zero. The inductance current flows through the freewheeling diode of S_1 until it reaches zero. Then, the inductance current continues to increase with the same inclination and reaches $i_{Llk}(t_1)$ value. Meantime, the inductance current flows through S_1. Q_2 turns off at t_1 and Mode_0 is completed.

Mode_1 ($t_1 - t_2$ time interval): Operating period of Mode_1 is $(0.5 - D)T_{sw}$; starts with Q_2 turning off and ends with Q_1 and Q_3 turning on as illustrated in Fig. 2. At t_1, Q_2 turns off. Q_4 has already turned on until the end of Mode_1. The secondary referred inductance current flows through Q_4 and the freewheeling diode of Q_3 until the period of Mode_1. The new active current path generated with Q_2 turning off and its reduced circuit diagram are shown in Figs. 3(b-1) and (b-2), respectively. $v_{ab}(t)$ voltage in Mode_1 is the same as Mode_0 because the positions of the switches in the primary side do not change in Mode_1. The primary referred value of $v_{cd}(t)$ becomes zero with Q_2 turning off. Therefore, as soon as Q_2 turns off, the inductance voltage becomes $(V_i/2)$ as illustrated in Fig. 2. The inductance current is positive, and its value is equal to $i_{Llk}(t_1)$ at t_1. After that time, the inductance current increases by $(V_i/2L_{lk})$ inclination and reaches to $i_{Llk}(t_2)$. Q_1 and Q_3 turn on at t_2, and Mode_1 is completed.

Mode_2 ($t_2 - t_3$ time interval): Operating period of Mode_2 is $(D - \delta)T_{sw}$; starts with Q_1 and Q_3 turning on and Q_4 turning off and

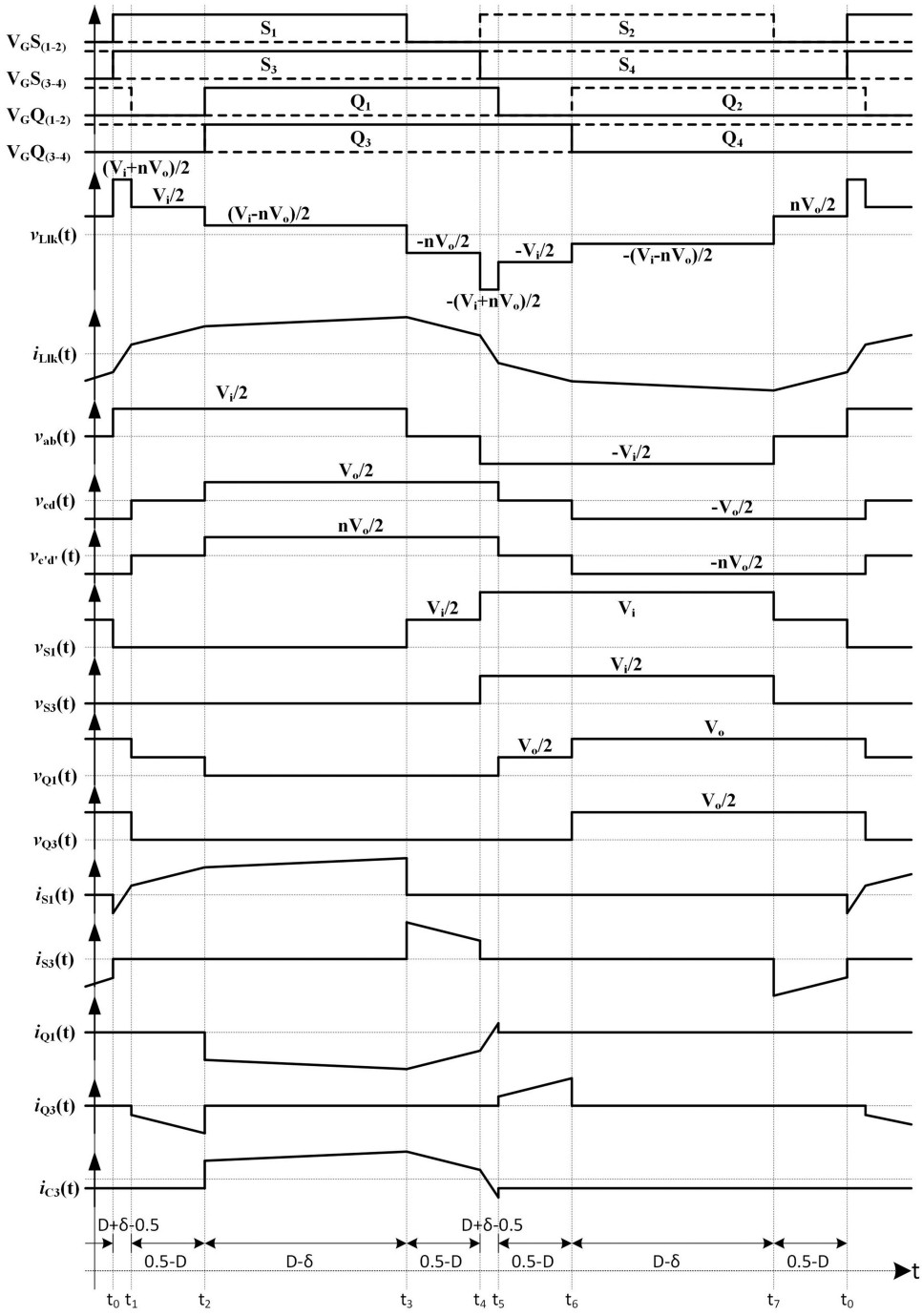


Fig. 2 *Voltage and current waveforms of switching devices, bridges and leakage inductance in CCM operation*

ends with S_1 turning off, as illustrated in Fig. 2. The secondary referred inductance current flows through the freewheeling diode of Q_1 and is transferred to load and C_3 with Q_4 turning off. The new active current path generated with Q_4 turning off and its reduced circuit diagram is shown in Figs. 3(c-1) and (c-2), respectively. $v_{ab}(t)$ voltage in Mode$_2$ is the same as Mode$_1$ because the positions of the switches in the primary side do not change in Mode$_2$. The primary referred value of $v_{cd}(t)$ becomes $(nV_o/2)$ with Q_4 turning off. Therefore, as soon as Q_4 turns off, the inductance voltage becomes $(V_i - nV_o/2)$ as illustrated in Fig. 2. When Q_4 turns off at t_2, the inductance current is positive and its value equal to $i_{Llk}(t_2)$. If V_i is greater than V_o, then the inductance voltage is positive. In this case, the inductance current increases by positive $((V_i - nV_o)/(2L_{lk}))$ inclination and reaches to $i_{Llk}(t_3)$. If V_i is less than V_o, the inductance voltage is negative. In this case, the inductance current decreases by negative $((V_i - nV_o)/(2L_{lk}))$ inclination and reaches the $i_{Llk}(t_3)$. S_1 turns off at t_3, and Mode$_2$ is completed.

Mode$_3$ ($t_3 - t_4$ *time interval*): Operating period of Mode$_3$ is $(0.5 - D)T_{sw}$; starts with S_1 turning off, and ends with S_3 turning off and S_2 and S_4 turning on, as illustrated in Fig. 2. S_1 turns off at t_3, and S_3 has already turned on until the end of Mode$_3$. The inductance current flows through S_3 and the freewheeling diode of S_4 when S_1 turned off. The new active current path generated with S_1 turning off and its reduced circuit diagram is shown in Figs. 3(d-1) and (d-2), respectively. $V_{cd}(t)$ in Mode$_3$ is the same as Mode$_2$ because the positions of the switches in the secondary side are the same. $V_{ab}(t)$ becomes zero with S_1 turning off. Therefore, as soon as S_1 turned off, the inductance voltage becomes $-(nV_o/2)$ as illustrated in Fig. 2. The moment when S_1 turned off at t_3, the inductance current is positive and its value is equal to $i_{Llk}(t_3)$. After that time, the inductance current decreases by $-(nV_o/2L)$ inclination and reaches to $i_{Llk}(t_4)$. S_3 turns off, and S_2 and S_4 turn on at t_4, and Mode$_3$ is completed. The second half period begins at t_4. The operating principle of this new period is the same as Mode$_0$, Mode$_1$, Mode$_2$, Mode$_3$; only the sign of the current and voltage

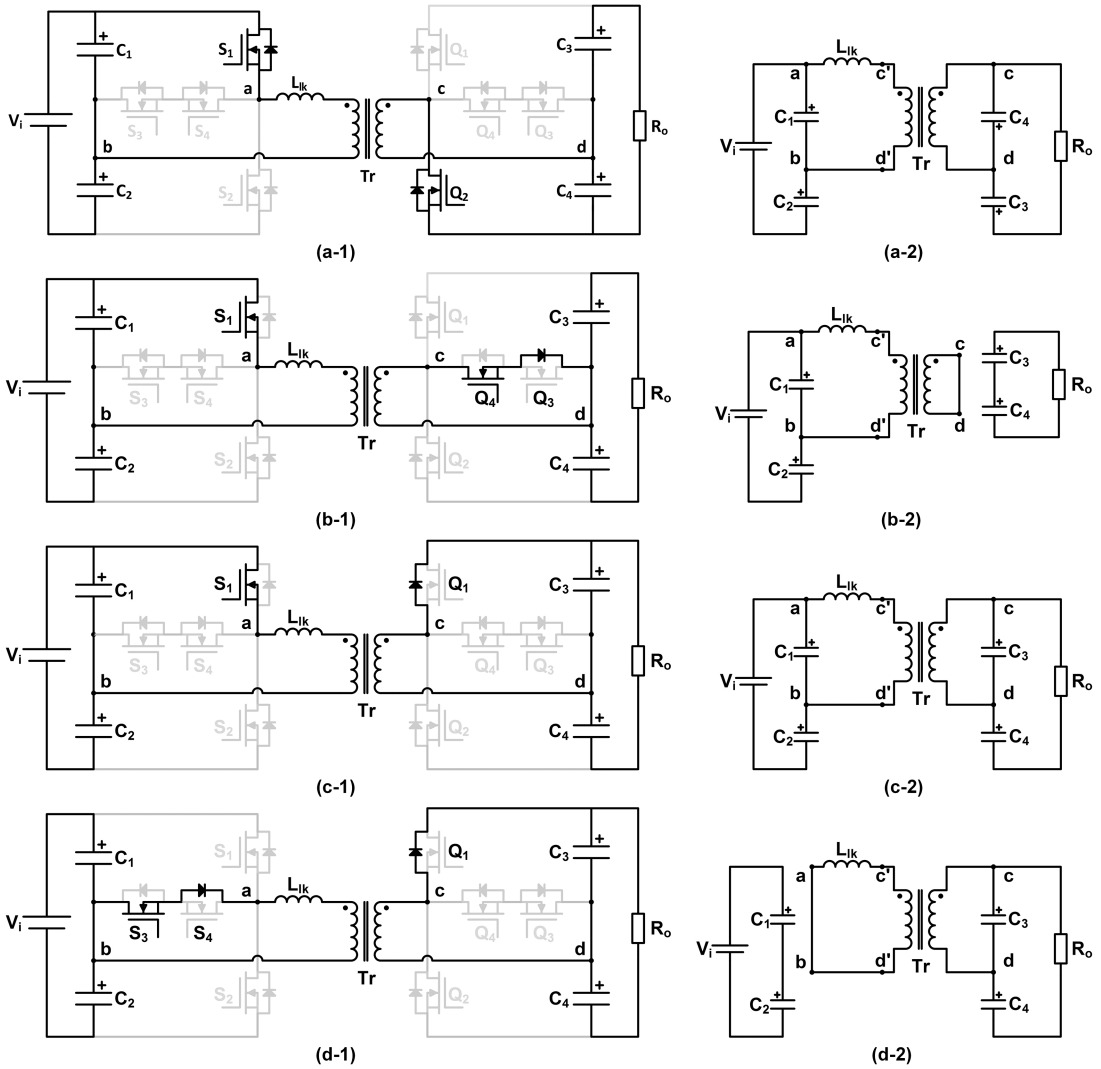


Fig. 3 *Active current paths and its reduced circuits for*
(a) Mode0, ***(b)*** Mode1, ***(c)*** Mode2, ***(d)*** Mode3

signals is different. Therefore, only the first half period has explained in this paper.

2.4 DC voltage gain for CCM operation

The DC voltage gain, M_{VDC}, of the proposed converter can be found by capacitor charge balance principle of one of the output capacitors. According to the capacitor charge balance principle, the averaged current of a capacitor is equal to zero over one switching period.

In this paper, the output capacitor C_3 is selected to calculate M_{VDC}. The current waveform of C_3 is illustrated in Fig. 2 and its averaged value can be expressed as

$$\int_0^{T_{\mathrm{sw}}} i_{C3}(t)\mathrm{d}t = \int_0^{T_{\mathrm{sw}}} -i_{Q1}(t)\mathrm{d}t - \int_0^{T_{\mathrm{sw}}} i_{\mathrm{o}}(t)\mathrm{d}t = 0 \tag{1}$$

where $i_{Q1}(t)$ can be calculated using the current–voltage characteristic of the leakage inductance for each sub-mode which is explained previous part and can be written as follows

$$\Delta I_{\mathrm{Llk(MODE_0)}} = i_{\mathrm{Llk}}(t_1) - i_{\mathrm{Llk}}(t_4) = \frac{V_i + nV_{\mathrm{o}}}{2L_{\mathrm{lk}}}(D + \delta - 0.5)T_{\mathrm{sw}} \tag{2}$$

$$\Delta I_{\mathrm{Llk(MODE_1)}} = i_{\mathrm{Llk}}(t_2) - i_{\mathrm{Llk}}(t_1) = \frac{V_i}{2L_{\mathrm{lk}}}(0.5 - D)T_{\mathrm{sw}} \tag{3}$$

$$\Delta I_{\mathrm{Llk(MODE_2)}} = i_{\mathrm{Llk}}(t_3) - i_{\mathrm{Llk}}(t_2) = \frac{V_i - nV_{\mathrm{o}}}{2L_{\mathrm{lk}}}(D - \delta)T_{\mathrm{sw}} \tag{4}$$

$$\Delta I_{\mathrm{Llk(MODE_3)}} = i_{\mathrm{Llk}}(t_4) - i_{\mathrm{Llk}}(t_3) = -\frac{nV_{\mathrm{o}}}{2L_{\mathrm{lk}}}(0.5 - D)T_{\mathrm{sw}} \tag{5}$$

Note that, D is the duty cycle of the main power switches (S_1, S_2, Q_1, Q_2). The expressions of the leakage inductance current of t_1, t_2, t_3, t_4 time can be written using (2)–(5) as follows

$$i_{\mathrm{Llk}}(t_1) = \frac{1}{4L_{\mathrm{lk}}f_{\mathrm{sw}}}\{D(V_i + nV_{\mathrm{o}}) + (2\delta - 1)V_i\} \tag{6}$$

$$i_{\mathrm{Llk}}(t_2) = \frac{1}{4L_{\mathrm{lk}}f_{\mathrm{sw}}}\{DnV_{\mathrm{o}} + (2\delta - D)V_i\} \tag{7}$$

$$i_{\mathrm{Llk}}(t_3) = \frac{1}{4L_{\mathrm{lk}}f_{\mathrm{sw}}}\{DV_i + (2\delta - D)nV_{\mathrm{o}}\} \tag{8}$$

$$i_{\mathrm{Llk}}(t_4) = \frac{1}{4L_{\mathrm{lk}}f_{\mathrm{sw}}}\{D(V_i + nV_{\mathrm{o}}) + (2\delta - 1)nV_{\mathrm{o}}\} \tag{9}$$

The values of $i_{Q1}(t)$ at t_2, t_3, t_4, t_5 can be calculated using (6)–(9). The average value of $i_{Q1}(t)$ can then be calculated by geometric methods using the instantaneous values at t_2, t_3, t_4 and t_5. Note that, $i_{\mathrm{Llk}}(t_5)$ is equal to $-i_{\mathrm{Llk}}(t_1)$. In addition, the average value of $i_{\mathrm{o}}(t)$ can be expressed as (V_{o}/R_0). The average value of $i_{C3}(t)$ for CCM operation can be calculated as the sum of the average values of

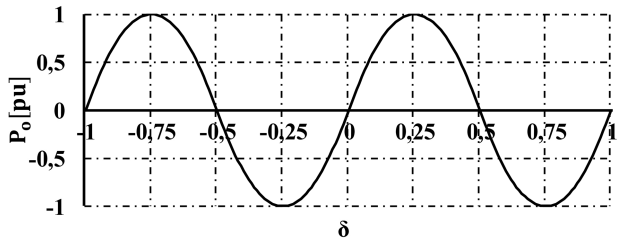


Fig. 4 *Output power (P_o) versus phase shift ratio (δ)*

$i_{Q1}(t)$ and $i_o(t)$ currents as expressed in (1). So, the voltage gain of the proposed converter for CCM operation can be calculated using the charge balance principle of C_3 as follows

$$M_{VDC} = \frac{R_o}{4nL_{lk}f_{sw}}\{D(1-D) + \delta(1-2\delta) - 0.25\} \quad (10)$$

Meantime, the phase shift ratio (δ) can be written in terms of parameters of the converter as

$$\delta = \frac{1 - \sqrt{-8D^2 + 8D - ((32nL_{lk}f_{sw}MV_{DC})/R_o) - 1}}{4} \quad (11)$$

2.5 Power transfer characteristic

The power transferred from the transformer can be found by using primary side current and voltage of the isolation transformer as the output power of the ideal converter. $V_{ab}(t)$ and $V_{c'd'}(t)$ voltages of the converter can be calculated using Fourier transformation as follows

$$V_{ab}(t) = \sum_{k=1}^{\infty}\{V_i b_k \sin(k\omega t)\} \quad (12)$$

$$V_{c'd'} = \sum_{k=1}^{\infty}\{nV_o b_k \sin[k(\omega t - 2\pi\delta)]\} \quad (13)$$

where b_k is the Fourier coefficient, and it is calculated as

$$b_k = \frac{\left[(-1)^k - 1\right]}{k\pi}\cos[k(0.5 - D)\pi] \quad (14)$$

The voltage value across the leakage inductance is calculated using (12) and (13) as follows in (15).

$$V_{Llk}(t) = \sum_{k=1}^{\infty} b_k\sqrt{V_i^2 + (nV_o)^2 - 2V_i nV_o\cos(2\pi k\delta)}\sin(k\omega t + \theta) \quad (15)$$

Where θ is the phase of the inductance voltage, and it is calculated as

$$\angle V_{Llk} = \theta = \arctan\frac{nV_o\sin(2\pi k\delta)}{V_i - nV_o\cos(2\pi k\delta)} \quad (16)$$

The current value of the leakage inductance is calculated as

$$I_{Llk}(t) = \frac{V_{Llk}(t)}{Z_{Llk}} \quad (17)$$

where Z_{Llk} is the leakage impedance according to each harmonic component, and it is calculated as

$$Z_{Llk} = k\omega L_{lk} \quad (18)$$

The current value of the leakage inductance can be calculated using (15) and (18) as follows in (19).

$$I_{Llk}(t) = \sum_{k=1}^{\infty} b_k\frac{1}{k\omega L_{lk}}\sqrt{V_i^2 + (nV_o)^2 - 2V_i nV_o\cos(2\pi k\delta)}*\sin\left(k\omega t + \theta - \frac{\pi}{2}\right) \quad (19)$$

As a result, the output power of the proposed converter can be calculated using (13) and (19) as follows in (20).

$$P_o = \frac{1}{2}\sum_{k=1}^{\infty} b_k^2\frac{nV_o}{k\omega L_{lk}}\sqrt{V_i^2 + (nV_o)^2 - 2V_i nV_o\cos(2\pi k\delta)}*\cos\left(-2\pi k\delta - \theta + \frac{\pi}{2}\right) \quad (20)$$

The direction and size of the output power can be changed by varying δ between −1 and +1 theoretically as shown in Fig. 4. However, the direction and size of the output power for $-1 \le \delta \le -0.5$ and $0.5 \le \delta \le 1$ are the same as $0 \le \delta \le 0.5$ and $-0.5 \le \delta \le 0$, respectively. Therefore, it is sufficient to change δ between −0.5 and 0.5 in order to change the direction and size of the output power. As seen in Fig. 4, the phase shift ratio of the converter can be selected between −0.25 and 0.25, as it is sufficient to transfer the maximum power in the forward or reverse direction for the range $-0.5 \le \delta \le 0.5$. Namely, the direction and size of the output power in full load range can be controlled by varying the phase shift of the bridges between $-\pi/2$ and $\pi/2$.

2.6 Calculation of maximum leakage inductance

The phase shift ratio of the converter must set to its maximum value of $|\delta_{max}| = 0.25$, in order to transfer maximum power in forward or reverse direction, as seen in Fig. 4. Thus, the maximum inductance value that can be used to transfer the requested maximum power from the converter is calculated using (20) as follows in (21).

$$L_{lk(max)} = \frac{1}{2}\sum_{k=1}^{\infty} b_k^2\frac{nV_o}{k\omega P_{o(max)}}\sqrt{V_i^2 + (nV_o)^2 - 2V_i nV_o\cos\left(k\frac{\pi}{2}\right)}*\cos\left(-2\pi k\frac{\pi}{2} - \theta + \frac{\pi}{2}\right) \quad (21)$$

2.7 Calculation of critical leakage inductance

The critical leakage inductance value can be found from the BCM mode of the converter. t_4–t_5 time interval in Fig. 2 must be equal to zero if the converter is in BCM mode. So, the expression of δ for the converter in BCM mode can be written as

$$\delta = 0.5 - D \quad (22)$$

The average value of the $i_{Q1}(t)$ is equal to I_o for each mode of operation, including BCM. Furthermore, the inductance current is equal to zero at t_4 for BCM. Thus, the average value of the $i_{Q1}(t)$ is calculated as

$$\int_0^{T_{sw}} i_{Q1}(t)\mathrm{d}t = \frac{i_{Llk}(t_2)+i_{Llk}(t_3)}{2}(D-\delta)+\frac{i_{Llk}(t_3)}{2}(0.5-D)=I_o \quad (23)$$

Now, the critical leakage inductance is calculated when (7), (8) and (22) are inserted in (23) as

$$L_{Lk_{crt}} = \frac{(-10V_i - 2nV_o)D^2 + (7V_i + nV_o)D - V_i}{16I_o f_{sw}} \quad (24)$$

3 Simulation study

The validation of the presented theoretical calculations is provided in this section using the PSIM simulation software. The design parameters used in this simulation study are presented in Table 1.

Figs. 5*a* and *b* show the simulation diagram of the control circuit and power circuit, respectively. Similar to theoretical analysis, all circuit elements are considered ideal during the simulations. There are four inputs to the control circuit; 'D', 'fsw', 'phs' and 'td'. D is the duty cycle of the $S_1 - S_2$ and $Q_1 - Q_2$; fsw is the switching frequency; phs is the phase shift between the driving signals of $S_1 - Q_1$, $S_2 - Q_2$, $S_3 - Q_3$, $S_4 - Q_4$ and it is 2π times of the phase shift ratio (δ) and td is the switching delay. Using the values in Table 1, the maximum value of leakage inductance is calculated as 50 µH via (21) and the critical inductance value is calculated as 31.2 µH via (24) by taking into account a minimum 35% load condition and 47% duty cycle. The inductance value used in the simulation study is selected as 35 µH, so that it remains between minimum and maximum inductance values. Furthermore, δ is calculated as 0.1177 for the output power of 2 kW using (11), which results in phs to be calculated as 0.7396 radians.

Fig. 6 shows the simulation results of the converter. In Fig. 6*a*, VG_S1, VG_S2, VG_Q1, VG_Q2 are gating signals of the related switches and V_AB, V_CD are the bridge voltages of the converter and V_Llk and I_Llk is the voltage and current of the inductor, respectively. Fig. 6*a* shows that primary and secondary bridge voltages have three-level voltage waveform and inductor voltage has a multi-level voltage waveform. In Fig. 6*b*, V_S1, V_Q1, V_S3, V_Q3 and I_S1, I_Q1, I_S3_S4, I_Q3_Q4 are the voltages and currents of the related switches, and V_o is the output voltage of the converter. Fig. 6*b* shows that the voltage on the primary and secondary side main switches are equal to the input and output voltages, respectively, whereas the voltage on the auxiliary switches is half of the input and output voltages. Also, as shown in Fig. 6*b*, the output voltage reaches 400 V for calculated δ value according to the output power of 2 kW. As a result, the simulation outputs validate theoretical calculations and analysis presented in the previous section.

4 Experimental study

Experimental validation of the developed converter is performed in this section by examining of current and voltage stress of the switches, current and voltage waveforms of the inductance, voltage gain and power transfer characteristics of the converter, and the efficiency of the converter in 20–100% load range. Furthermore, the switching transitions of the switches have been experimentally studied in this section. The experimental study of the developed

Table 1 Design parameters of the 3LTT-IBDC

Parameters	Symbols	Values
input voltage	V_i	400 V
output voltage	V_o	400 V
output power	P_o	2 kW
switching frequency	f_{sw}	50 kHz
voltage gain	$MV_{DC} = V_o/V_i$	1

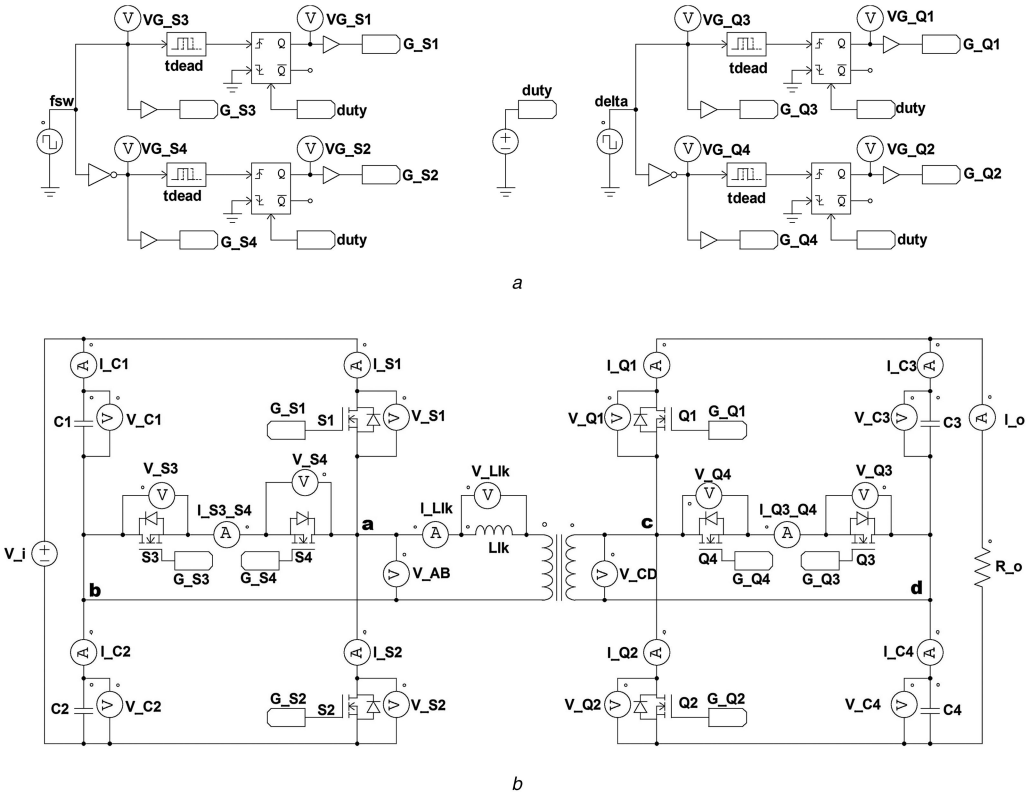
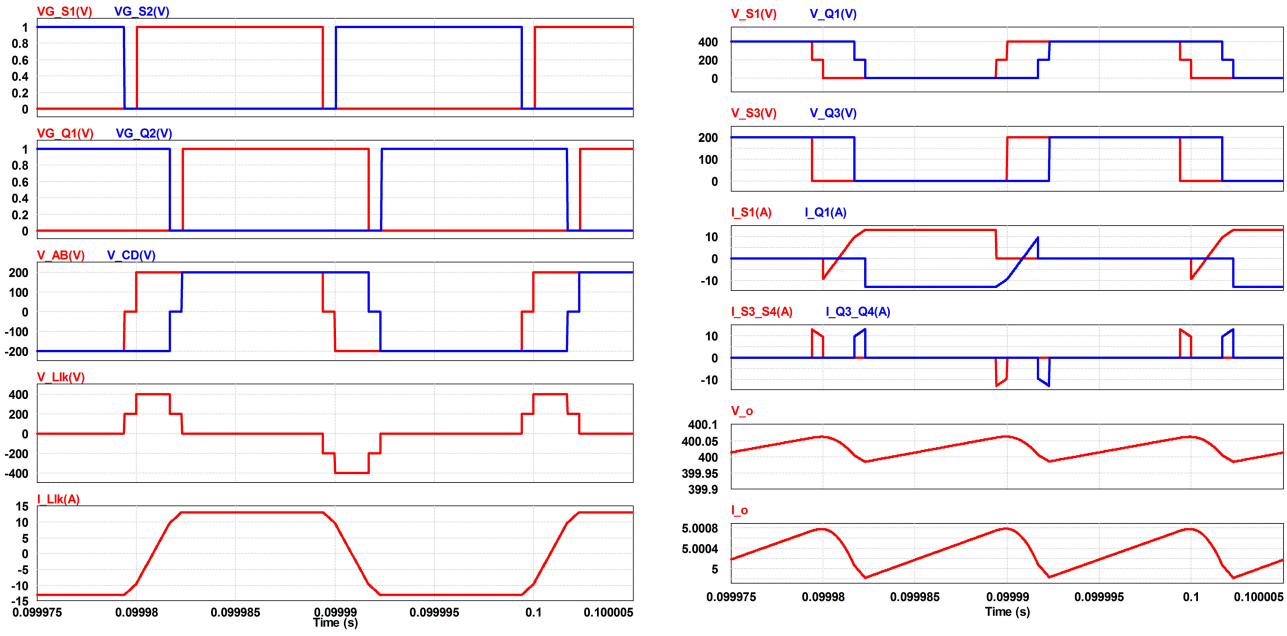


Fig. 5 *Simulation circuit of the 3LTT-IBDC*
(a) Control circuit, (b) power circuit



a *b*

Fig. 6 *Simulation results of the 3LTT-IBDC*

Table 2 Basic components of the prototype

parameters	Symbols	Values
transformer	Tr	$\frac{n_p}{n_s} = 1$, Epcos E65(N87), $L_m = 700\ \mu$H,
external inductance	L	$n = 43$, 35 μH, MP-157014-2
switches	$S_1, S_2, S_3, S_4, Q_1, Q_2, Q_3, Q_4$	FCH47N60F Fairchild
input and output capacitors	C_1, C_2, C_3, C_4	3 × 100 μF/250 V Electrolytic

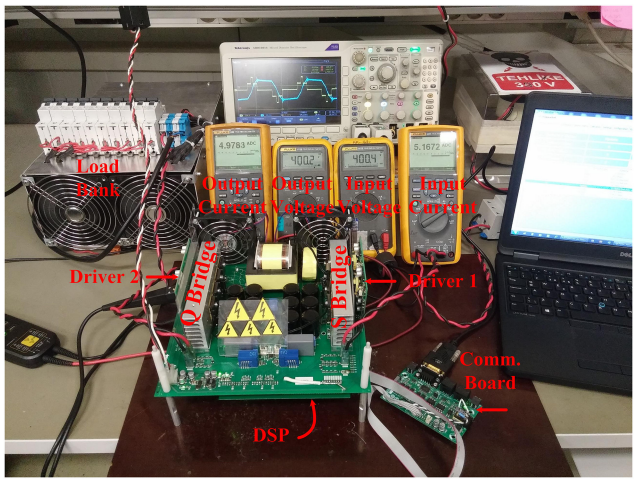


Fig. 7 *Prototype of the proposed converter*

3LTT-IBDC is performed by 2 kW prototype. Basic components of the prototype are given in Table 2.

The prototype consists of five sub-boards that are main power board, control board, communication board and two driver boards. The main power board contains semiconductor switches, isolation transformer, external inductance, input and output filter capacitors, heatsink and fans for cooling. The control board is designed using the C2000 TMS320F28377 Delfino series DSP by TI. The communication board has used the prototype to communicate with a PC via UART. Two isolated driver boards that have four independent voltage outputs are used to drive the switches on each bridge. The selection and design of circuit elements such as capacitors, coils, and transformers used in the prototype affect the efficiency of the proposed converter. Selecting capacitors with low ESR is beneficial for efficiency. Therefore, the capacitors are selected from the low ESR series (B43896) of EPCOS. It is also aimed to reduce the ESR effect by paralleling the capacitors. On the other hand, type and size of a magnetic material and cross-sectional area of a conductor used in a design of winding elements such as inductor and transformer will affect core and copper losses, respectively. So, they have been selected at the appropriate values according to the power of the transformer in the experimental study. The photography of the proposed converter is presented in Fig. 7.

The oscilloscope outputs of the constructed experimental study for full load condition are presented in Figs. 8 and 9. In Fig. 8*a*, channel 1 (dark blue) is gate signal of S_1, channel 2 (turquoise) is gate signal of Q_1, channel 3 (magenta) is voltage of the leakage inductance and channel 4 (green) is current of the leakage inductance. As seen in Fig. 8*a*, the voltage of inductance has a multi-level waveform. In Fig. 8*b*, channel 1 (dark blue) is gate signal of S_1, channel 2 (turquoise) is gate signal of Q_1, channel 3 (magenta) is $V_{ab}(t)$ and channel 4 (green) is $V_{cd}(t)$. As seen in Fig. 8*b*, primary and secondary voltages have three-level voltage waveform. In Fig. 8*c*, channel 1 (dark blue) is gate signal of S_1, channel 2 (turquoise) is current of S_1, channel 3 (magenta) is a voltage of S_1 and channel 4 (green) is current of the leakage inductance. As seen in Fig. 8*c*, the voltage stress of S_1 is equal to the input voltage. In addition, the voltage stress drops to half of the input voltage before the switch S_1 is turned on and off. This reduces switching losses. In Fig. 8*d*, channel 1 (dark blue) is gate signal of S_3, channel 2 (turquoise) is current of S_3, channel 3 (magenta) is a voltage of S_3 and channel 4 (green) is current of the leakage inductance. As seen in Fig. 8*d*, voltage stress of S_3 is equal to half of the input voltage. Since the voltage stress of the switch S_3 is equal to half of the input voltage, the switching losses of S_3 can be low.

In Fig. 9*a*, channel 1 (dark blue) is gate signal of Q_1, channel 2 (turquoise) is current of Q_1, channel 3 (magenta) is voltage of Q_1 and channel 4 (green) is current of the leakage inductance. As seen in Fig. 9*a*, the voltage stress of Q_1 is equal to the output voltage; however, the voltage stress at the moment of switching is half of the output voltage. In Fig. 9*b*, channel 1 (dark blue) is gate signal of Q_3, channel 2 (turquoise) is current of Q_3, channel 3 (magenta) is voltage of Q_3 and channel 4 (green) is current of the leakage inductance. As seen in Fig. 9*b*, the voltage stress of Q_3 is equal to

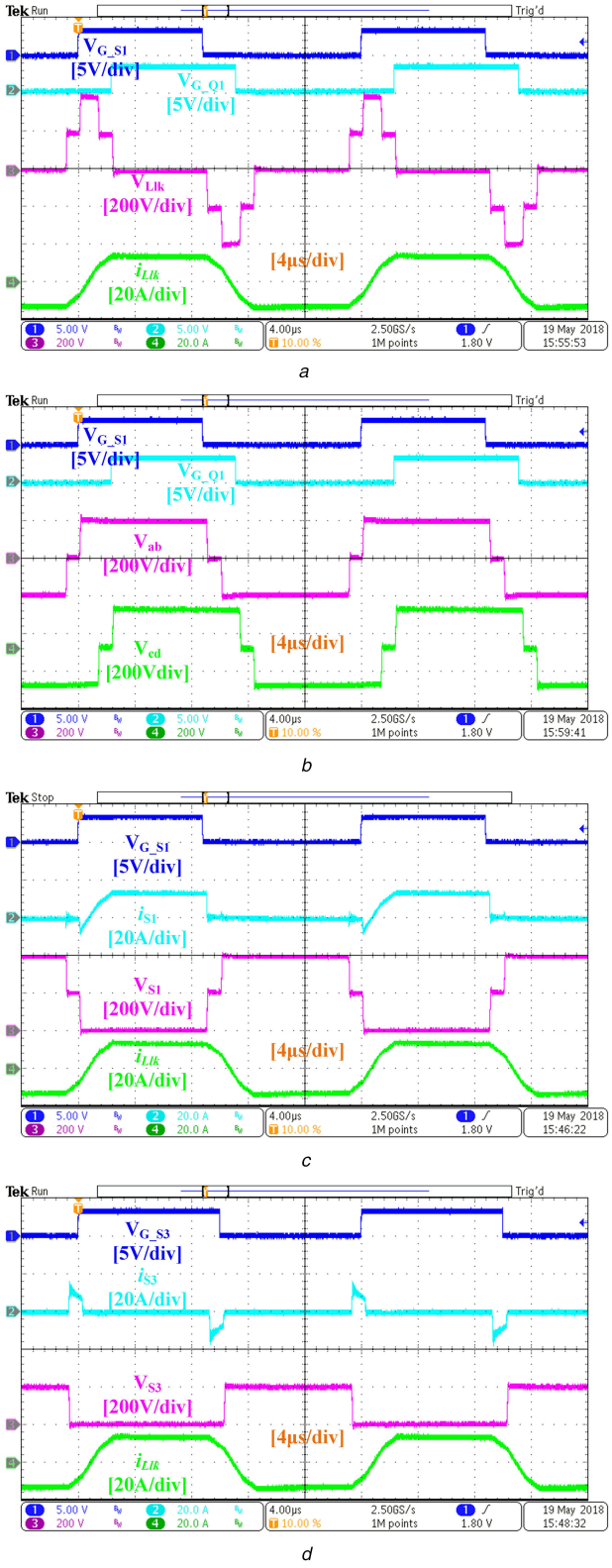


Fig. 8 *Waveforms of the prototype at full load condition*

(a) Inductance voltage (ch3) and current (ch4), ***(b)*** Primary (ch3) and secondary (ch4) bridge voltages, ***(c)*** current (ch2) and voltage (ch3), ***(d)*** current (ch2) and voltage (ch3)

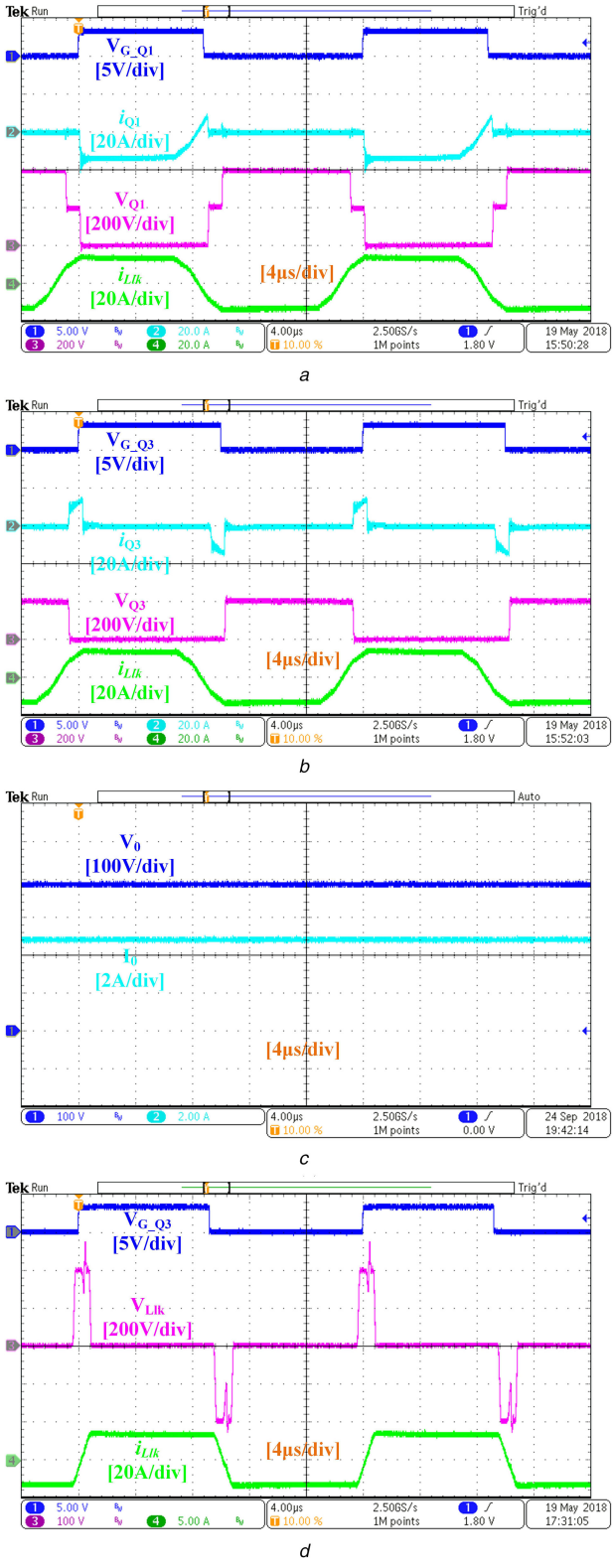


Fig. 9 *Waveforms of the prototype*

(a) Q_1 current (ch2) and voltage (ch3) at full load, ***(b)*** Q_3 current (ch2) and voltage (ch3) at full load, ***(c)*** Output voltage (ch1) and current (ch2) at full load, ***(d)*** Inductance voltage (ch3) and current (ch4) for BCM condition

half of the output voltage. Fig. 9*c*, channel 1 (dark blue) is output voltage (V_o) waveform and channel 2 (turquoise) is the output current (I_o) waveform. In this case, the input and output voltages are 400 V, the output current is about 5 Å. The applied phase shift ratio is 0.11175. In Fig. 9*d*, channel 1 (dark blue) is gate signal of S_1, channel 3 (magenta) is voltage of the leakage inductance in BCM mode, and channel 4 (green) is current of the leakage inductance in BCM mode. In this case, the input and output voltages are 400 V. The applied phase shift ratio (δ) is 0.034. As seen in Fig. 9*d*, the leakage inductance current is in the boundary between the continuous conduction and discontinuous conduction at 35% load condition.

The efficiency analysis of the prototype is presented in Fig. 10. Four high-resolution multimeters are used to measure the input and the output currents and voltages for efficiency measurements. Efficiency measurements are taken simultaneously by photographing for the accuracy of the results. The measured maximum efficiency of the prototype is 96.81 at 70% load

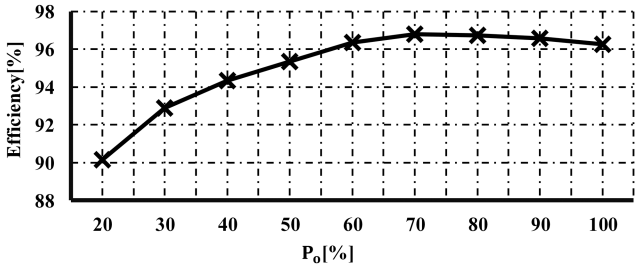


Fig. 10 *Efficiency analysis of the proposed converter*

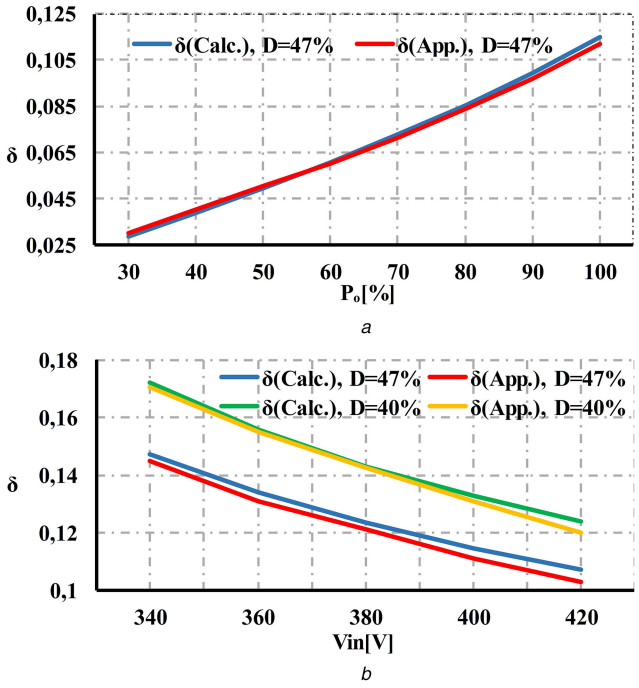


Fig. 11 *Power transmission and input voltage characteristics*

(a) Relationship between calculated and applied δ at different power levels for $D = 47\%$, ***(b)*** Relationship between calculated and applied δ at different input voltages for $D = 47\%$ and $D = 40\%$

condition and the measured minimum efficiency is 90.15 at 20% load condition as illustrated in Fig. 10. Furthermore, the measured efficiency of the prototype is 96.27% at full load condition. The peak efficiencies of 94.8% at 2.8 kW [24], 95.5% at 1.2 kW [25], 96.5% at 1.2 kW [26], 96.71% at 1 kW [16] can be found in the literature of three-level isolated bidirectional DC–DC converters. Therefore, the proposed 3LTT-IBDC seems more promising in terms of achieving high efficiency.

Fig. 11*a* shows the relationship between calculated δ by (11) and applied δ in the experimental study for the different load conditions. In the experimental study, the power transfer characteristic of the converter is analysed by applying the δ value to the converter, which provides an output voltage of 400 V at each load stage with an input voltage of 400 V. Fig. 11*b* shows the relationship between calculated δ by (11) and applied δ for different input voltage and two different D conditions in the experimental study. In this case, the δ values of the converter for each duty cycle are analysed by increasing the input voltage at 20 V intervals starting at 340 V at full load condition. According to the analysis results, the calculated δ values and applied δ values for the different input voltages and duty cycles are largely overlapping. While performing the theoretical analysis of the proposed converter, it is expected that there will be slight differences between the calculated and applied δ values since the circuit elements are considered as ideal.

Switching transition of the switches measured from the prototype is presented in Figs. 12 and 13. In the figures, channel 1 (dark blue) is gate signal of the corresponding switch, channel 3 (magenta) is voltage of the corresponding switch and channel 4

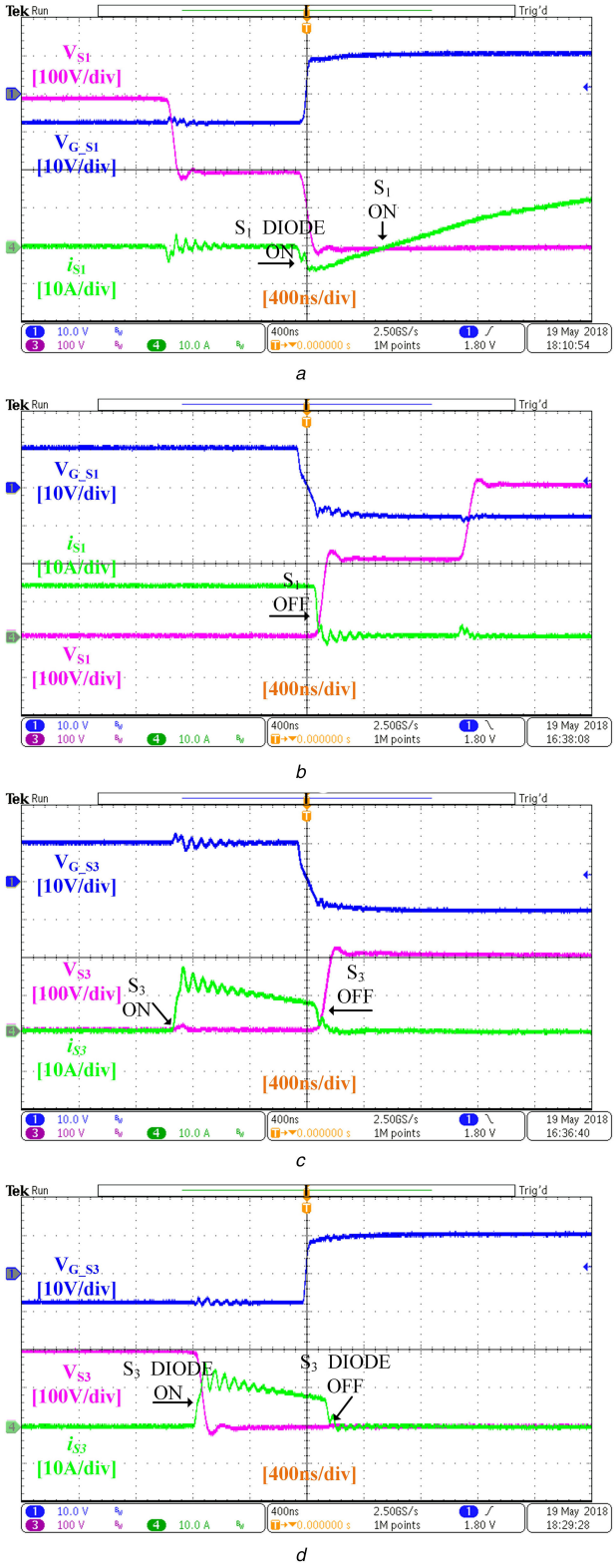


Fig. 12 *Switching transitions of the primary switches at full load condition*

(a) S_1 turning on, ***(b)*** S_1 turning off, ***(c)*** S_3 turning on and off, ***(d)*** S_3's freewheeling diode turning on and off

(green) is current of the corresponding switch. Fig. 12*a* shows that hard switching occurs when S_1's freewheeling diode turns on and the voltage of S_1 becomes zero when the inductance current flows through S_1. Fig. 12*b* shows that partially soft switching occurs when S_1 turns off. Fig. 12*c* shows that full soft switching and partial soft switching occur when S_3 turns on and off, respectively. Fig. 12*d* shows that hard and full soft switching occur when S_3's freewheeling diode turns on and off, respectively. Fig. 13*a* shows

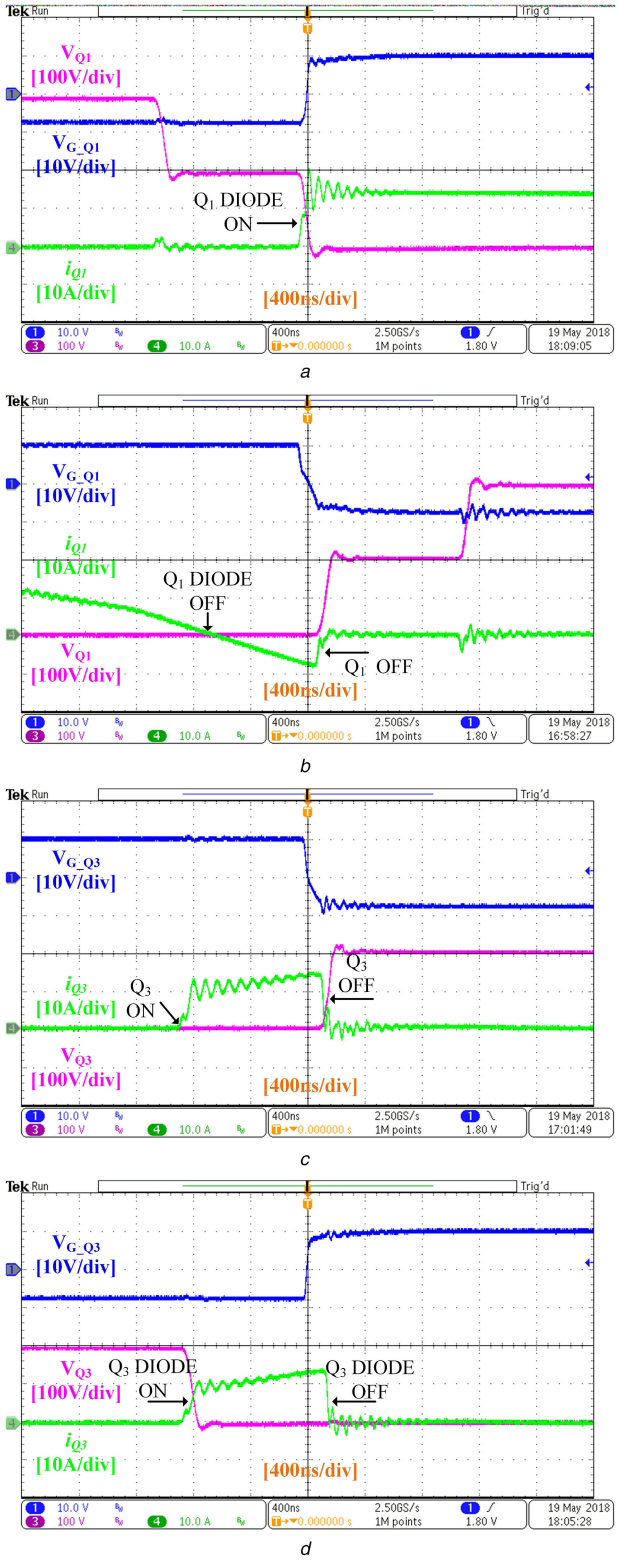


Fig. 13 *Switching transitions of the secondary switches at full load condition*

(a) Q_1's freewheeling diode turning on, ***(b)*** Q_1's freewheeling diode turning off, ***(c)*** Q_3 turning on and off, ***(d)*** Q_3's freewheeling diode turning on and off

that hard switching occurs when Q_1's freewheeling diode turns on. Fig. 13*b* shows that soft switching occurs when Q_1's freewheeling diode turns off. Fig. 13*c* shows that full soft switching and partial soft switching occurs when Q_3 turns on and off, respectively. Fig. 13*d* shows that hard and full soft switching occurs when Q_3's freewheeling diode turns on and off, respectively.

In Fig. 14, the switching and conduction losses of switches S_1, S_3, Q_1, Q_3 are analysed at full load condition. The total power loss for these four switches is approximately 25 W. The switching

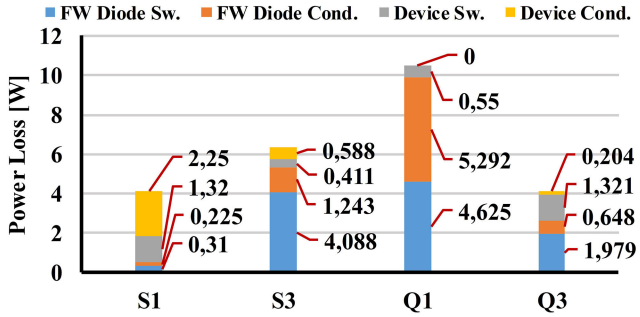


Fig. 14 *Loss analysis of the switches* (S_1, S_3, Q_1, Q_3)

and conduction losses of switches S_2, S_4, Q_2, Q_4 are approximately equal to ones of switches S_1, S_3, Q_1, Q_3. In this case, the total loss for all switches at full load condition is approximately 50 W. The losses of other circuit elements such as transformer, inductance and capacitors are about 27.5 W in total. The total power loss of the proposed converter for efficiency analysis is measured as 77.5 W.

5 Conclusion

The three-level T-type topology has been widely used in inverter and rectifier applications in recent years. This study presents a successful development and application of T-type topology in the isolated bidirectional DC–DC converter application. Theoretical, as well as simulation analysis of this novel converter and its performance validation with relevant experiments on a 2-kW prototype are presented in the paper. The presented results show that they were in good agreement with regards to representing the voltage gain, power transfer characteristic and the leakage inductance in BCM mode. In addition, the efficiency analysis of the developed converter is presented for various load conditions and a maximum efficiency of 96.8% is measured from the prototype.

This paper also investigates the switching transitions of switches of the 3LTT-IBDC, and hard, partially soft and full soft switching modes are identified during the operation. Further increases in converter efficiency by implementing a full soft switching mode to all the switches is aimed to be achieved in future studies.

6 Acknowledgment

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